Metallic Nanotransistors

by

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For my wife, Teresa, and my beloved daughter, Ashley...

Abstract

Efforts to downscale transistor dimensions to satisfy the demands for ultra high density integrated circuits have been met so far with optical lithography techniques. However, they are now facing their fundamental limits including optical diffraction and the limits associated with UV exposure sources. The feature size required for current integrated circuits is 45nm. In the near future it is predicted to reach 15nm node where conventional photolithography can no longer be employed. As a result, extensive research has been devoted into the development of next generation lithography processes and new transistor structures. Among the potential candidates for next generation transistor devices, nanowire based field effect structures made from a single layer of metal are proposed. These types of transistors are designed to operate similarly to a depletion type of MOSFET by governing the flow of electrons in a narrow nanowire channel.

In this study, metallic nanowire structures were designed, fabricated and tested. Nanowires with diameters as small as 12.5nm were fabricated using electron beam lithography (EBL), thermal evaporation and metal lift-off process. Optimisations of EBL parameters were made to deliver wires ranging from 200nm down to 12.5nm mainly by suppressing charging effects and minimising factors that contribute to proximity effects. These structures were the first in the Nanofabrication laboratory at the University of Canterbury to be fabricated with such dimensions. Nanowire structures in Y shaped and planar gated configurations have also been tested using Ag, Al, and NiCr.

Metallic nanowire devices were deposited on insulating substrates such as Si_3N_4 or SiO_2 to facilitate electrical characterisation and device operation. In the fabrication, the minimum achievable line widths is mainly determined by

the surface charging effects due to the direct EBL patterning on insulating substrates and by proximity effects for having gate structures located few tens of nanometres away from the main nanowire.

Electrical characterisations including two point, four point, transmission line measurements, and gate effects were performed using semiconductor parameter analyser to study the conduction and gating effect of these nanowires with gate electrodes that are separated by air gaps in the range of 20nm-200nm. The main challenging issues found to affect the characterisation results are the voltage offset problem during four point resistance measurement, the charge fluctuation and the effect of joule heating during long integration measurements.

To further study the gate effects of nanowires based on semi-metals, focused ion beam (FIB) technology was employed for the fabrication of bismuth nanotransistor structures, with minimum dimensions in the 30nm scale. In addition, we have for the first time report the creation of highly ordered and multiple layers of nano dots stacking using electron beam induced metal deposition in FIB.

In this thesis, although no significant gating effects were observed due to difficulties involved in further reducing the nanowire widths beyond the 12nm node, the fabrications and characterisations of these nanowire structures have allowed us to explore the resolution limits of these processes and at the same time create a platform suitable for studying the conduction characteristics, transport properties and the gate effects for nanowires made from semiconductor, metal and semimetal.

Acknowledgements

Throughout my PhD study I have received tremendous help and support from my supervisors, the research group, my colleagues, and my family. I would like to express my deepest appreciation to my supervisor, Assoc. Prof. Maan Alkaisi for his guidance and encouragement to this project. In fact, I was once disappointed with my progress and encountered bottlenecks for pushing the dimensions of nanowires into the 20nm regime. His patience and dedication to research have encouraged me countless times to take on these problems and proceed my research into the completion of this thesis today. I feel honoured to have him as my supervisor and mentor and will always remember the positive influence he has had on my life.

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Chapter 1

Introduction

In the world today, the continuous downscaling of solid state devices has been a major task for researchers and integrated circuit (IC) industries. The demands for higher performance, large storage capacity, low cost, and low power consumption computers were so high that the miniaturisation technology has in fact scaled down from 10μm to 45nm within the past five decades[15].

Most of the time, the scaling was simply carried out by reducing the feature size. However, a main challenge which lies ahead when the transistor feature size approaches the fundamental limits of the present pattern transfer technique is the photolithography. These limiting factors reflect the urge for new lithography solutions or devices based on new materials or structures. The motivation behind this project is to develop fabrication and replication processes for a new device design based on nanowires. These devices have been examined to explore and to analyse the physical and electrical properties of nanowire structures with potential for metallic nanoscale transistors.

We shall start by looking at the history of transistor development, the rapid evolution, and the fundamental limits for CMOS and conventional photolithography. Followed by the introduction to a few promising candidates for the next generation nanoscale transistor devices.

1.1 Development of transistor and modern computer

The advancement of technology has brought the society into the digital world today, where information is regularly processed and exchanged through platforms known as computers. The computers we use today are powerful and highly sophisticated as a result of improvement in transistor miniaturisation technology, a profound research that can be traced back to the beginning of twentieth century.

In 1906, Lee De Forest invented a three terminal vacuum device known as Audion, an electronic amplifier used in radio communication. It was not until 1925, the idea of field effect transistor devices (FET) was proposed by Julius Edgar Lilienfeld (Patented in 1930). Although his research in FET was of little interest and had no practical value due to the difficulties in extracting high purity semiconductor materials at that time. His original design of transistor has indeed paved the foundation of today's MOS technology.

During the period of 1939-1946, a number of computer devices have been built to perform logic, such as the famous Electronic Numerical Integrator And Computer (also known as ENIAC[16], as shown in Fig 1.1). These computer systems were huge, containing a large number of relays and short lived vacuum tubes which required frequent replacements.

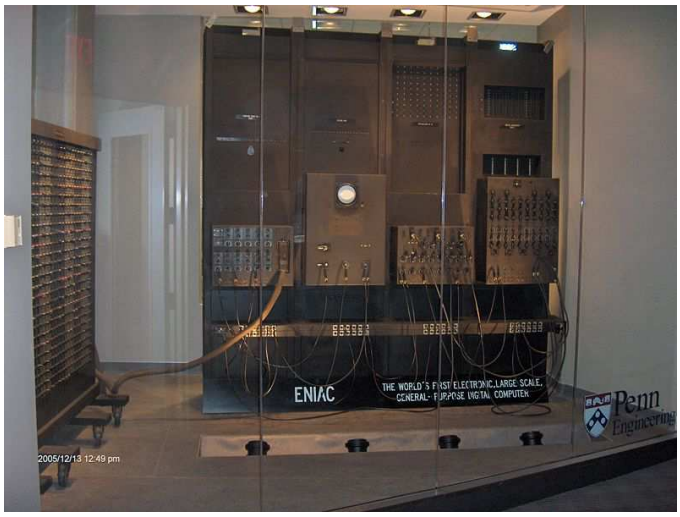
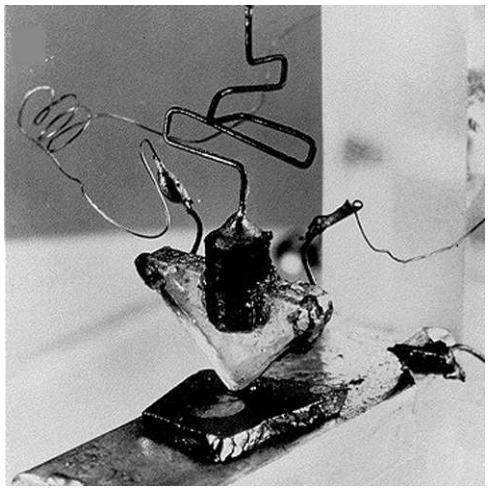
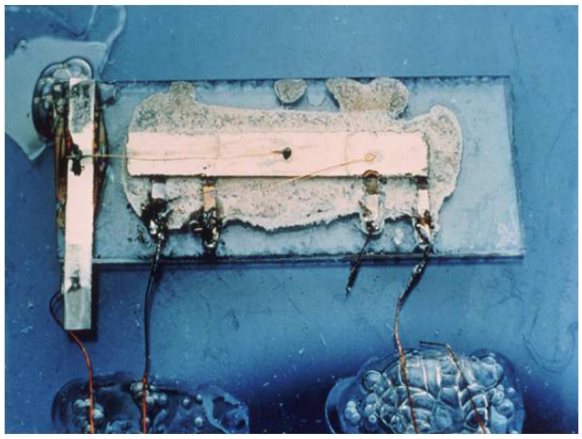


Figure 1.1: Part of the ENIAC system including four of its panels and one function tables on display at the University of Pennsylvania.

The revolution in microelectronics was initiated in 1947 when Bardeen, Brattain, and Shockley invented the first solid state transistor device[17]*, the bipolar junction transistor (BJT), as shown in Fig 1.2(a). Soon after its birth, in 1952, magnetic core memory was invented for replacing the bulky and short lived vacuum tube memories, making computer devices smaller and more reliable. Miniaturisation of computer chips was then made possible when the integrated circuit was invented by Kilby and Noyce for the integration of several BJTs on a single chip in 1959[18][19], as shown in Fig 1.2(b). Since then, the IC industry has undergone five decades of unprecedented and phenomenal growth.



(a) The world's first bipolar junction transistor (BJT)[17].



(b) The world's first IC: a transistor with resistors and capacitors on a single semiconductor chip[18].

Figure 1.2: Early transistor devices.

*Nobel prize Awarded in 1956.

In the 1960s, the fabrication processes for field effect transistor (FET) have become mature after Hofstein and Heiman developed the first FET[20]. FET based transistors outperformed BJT in terms of the integration area required, power consumption, and leakage current. They were later on integrated into Si chips as metal oxide semiconductor field effect transistors and subsequently complementary pair metal oxide semiconductor (CMOS) transistors within 10 years.

The CMOS technology has led to the development of the first commercial microprocessor, the Intel 4044 in 1971 [1]. This 4-bit processor contains 2300 MOS transistors, operating at 108 kHz, was designed for Busicom calculators. It was followed by the development of 8-bit, 16-bit, 32-bit processor and eventually 64 bit processors that allow for more complicated instructions and powerful calculations to be evolved and developed.

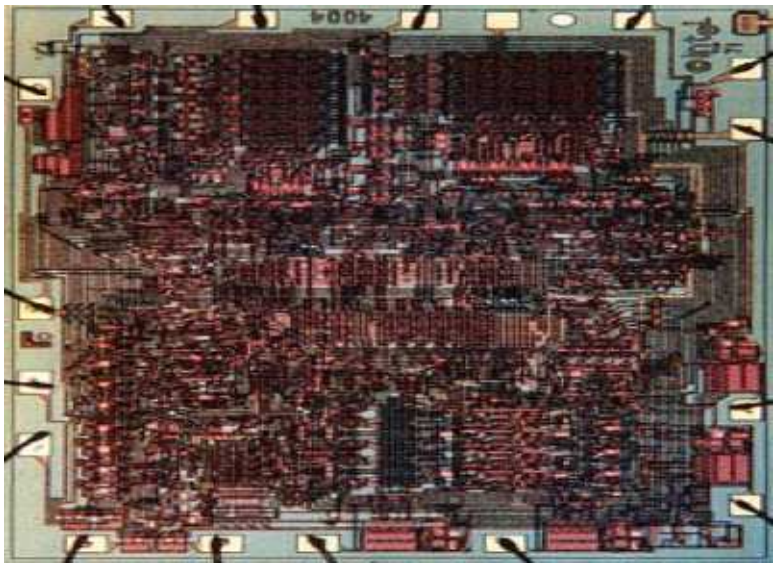


Figure 1.3: The first microprocessor, the Intel 4004 with 2300 transistors and 3mmx4mm size[1].

More and more transistors were integrated on a single chip since the development of the first microprocessor, where miniaturisation of transistors have become the dominant technology, leading to the cutting edge computers we have today. In 1965, Gordon Moore observed and predicted the growth of in-

tegration of IC chips, in which he stated the density, and the performance of integrated circuit will be doubled every two years[21]†. His prediction has been used extensively by IC manufacturers for processes bench marking and it has stayed unbeaten for four decades. Fig 1.4 shows Intel's strategy of continuous scaling of transistor feature size into the near future [2].

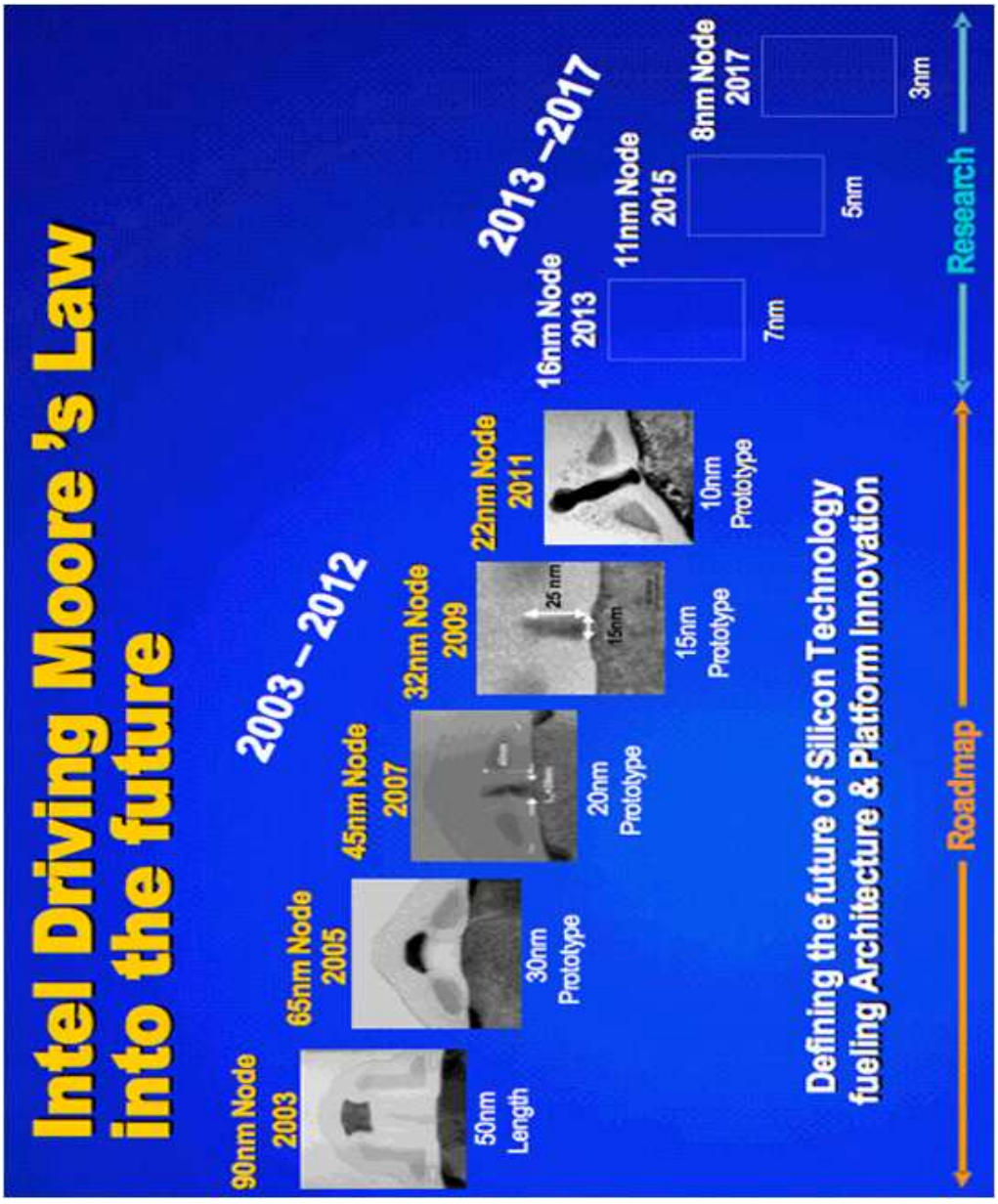


Figure 1.4: Transistor scaling: the continuum of reduced feature size, adapted from [2].

†It was revised again in 1974 based on the scaling rule set by Dennard in 1974[22].

1.2 CMOS limits and next generation transistors

The IC manufacturers have been following Moore's law closely[23]. Driven by the phenomenal advances in optical lithography, 45nm logic devices are now in high volume production and the prototype of 32nm node technology has already been fabricated by Intel[24]. The advantages of the miniaturisation of IC devices are the increase of overall performances and the decrease of cost per device, where the former is the direct result of reduced channel width that has shortened the traveling of carriers, and the later is the result of higher integration density.

1.2.1 CMOS limits

Year 2000 was the year when IC industry entered the nanometer era, where photolithography, the dominant technique used for pattern transfer transistor features onto Si wafers has began to face its fundamental limits[‡]. The main limiting factor is the diffraction, the effect of light diffracted or bent around the edge of a slit when the dimension of the slit is smaller than the wavelength of light passing through it. Fig 1.5 shows an example of optical diffraction, where the red light is significantly diffracted when passing through the feature size that is smaller than the wavelength of light. For blue light, the diffraction effect is less as the wavelength is smaller[25]. The diffraction limits have immediate effect on the resolution of photolithography, forcing semiconductor manufacturers to move to UV exposure sources with smaller and smaller wavelengths to keep up with the trend of scaling down. The cost involved in finding and implementing smaller wavelength light sources and their relevant optic systems is extremely expensive and can only provide short term solutions. As a result, the fate of conventional lithography is uncertain and it is likely to be replaced by next generation lithography techniques in the near future.

Enormous amount of research funding has been devoted into the development of the next generation lithography (NGL) processes and new types of nanoscale transistor devices. There exists a number of promising candidates for

[‡]The basic principles of photolithography will be covered in Chapter 3.

NGL including immersion lithography which replaces the airgap with a liquid medium[26][27], nanoimprint lithography (NIL)[28][29] that utilises a mold for stamping or printing of patterns on resists, extreme ultraviolet lithography[30] (EUV), and multiple beam lithography[31]. Other candidates such as dual beam focused ion beam lithography, Evanescent Near Field Optical Lithography (ENFOL)[32] have also received great interest over the last decade. In order to replace the current conventional photolithography technology, the new process must have high throughput, high resolution and a low cost of operation.

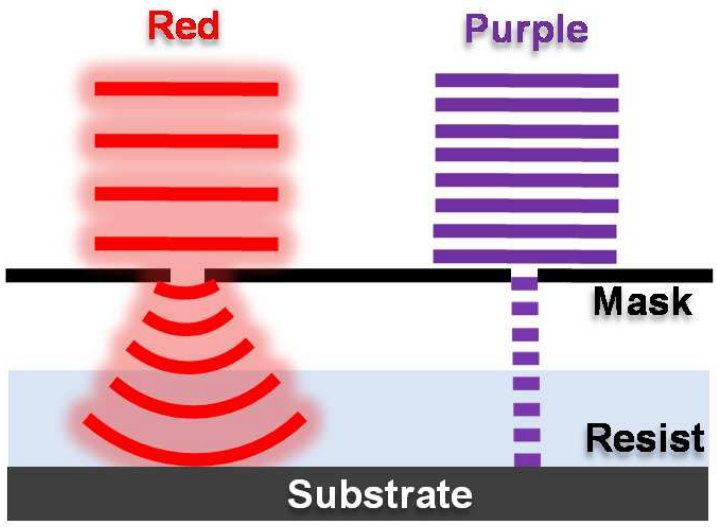


Figure 1.5: Diffraction of light: A simple example when light is diffracted when the wavelength is large than the feature size on a photomask.

In the meantime, immersion photolithography remains the most advanced lithography technique used by semiconductor manufacturers. The CMOS devices are also likely to face their practical limits such as short channel effects, and parasitic resistance and capacitance issues when the technology advances approaching the 20nm node[33][6][§]. As a result, new types of nanoscale transistor structures must be researched to replace the well established CMOS technology.

[§]The practical limits for CMOS transistors will be discussed in Chapter 2.

1.2.2 Next generation nanoscale transistors

In terms of the next generation nanotransistor devices, there are a number of candidates including single electron transistor (SET), carbon nanotube transistor, 1D graphene transistor, and nanowire transistors.

1.2.2.1 Single electron transistor

Single electron transistors are devices that operate by the tunneling of electrons. The tunneling in a single electron transistor can be precisely controlled by employing the mechanism of coulomb blockade, allowing only one electron to hop in or out of the Si island at a time by the applied gate voltage[34]. The coulomb blockade energy is the minimum energy required to transfer one electron onto the isolated island without the applied voltage. It can be described by the formula $\Delta E = e^2/2C$, where e is the charge of an electron, and C is the total capacitance of gate and tunnel junction[35]. Coulomb blockade can only be observed under two conditions. First, the energy of electrons due to thermal fluctuations must be much smaller than the coulomb energy, i.e. $\Delta E \gg kT$, where k is the Boltzman constant and T is the temperature in Kelvin. Secondly, the coulomb energy must be much greater than the electrochemical energy given by $\Delta E \gg eV$. SET can be implemented into digital logic circuits and memory devices by forming a series of arrays. Fig 1.6 shows a single electron inverter pattern on electron sensitive resist patterned using electron beam lithography. The design of this inverter was adapted and modified[¶] from Tucker[36], where the dimensions of tunneling islands were approximately 100nm in scale. For SETs, the uncontrollable charge fluctuations and low temperature operation are major obstacles for any real world application.

1.2.2.2 Carbon nanotube and 1D graphene transistor

Ever since the discovery of nanoscale carbon nanotubes, there has been great interest in applying this material into electronic devices. Carbon nanotubes are

[¶]The planar gates were modified into lateral gates for the ease of fabrication and replication.

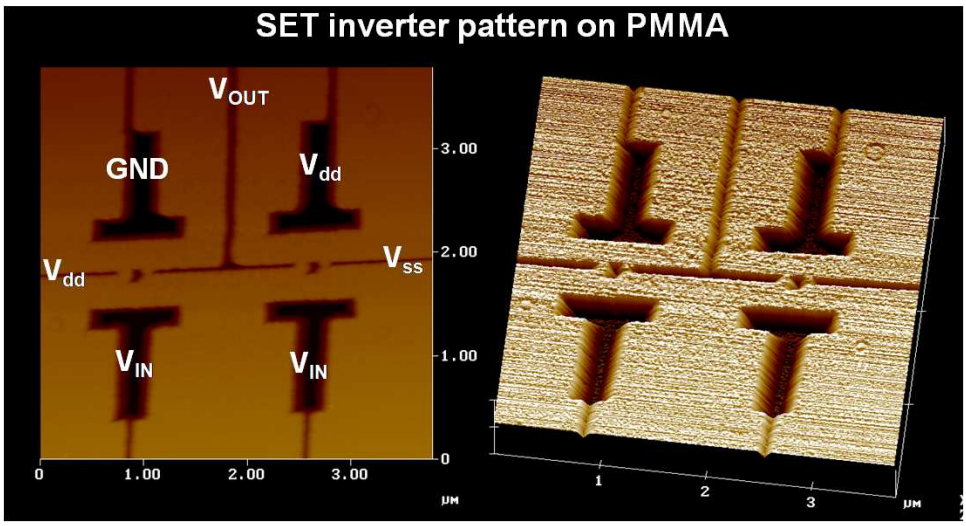
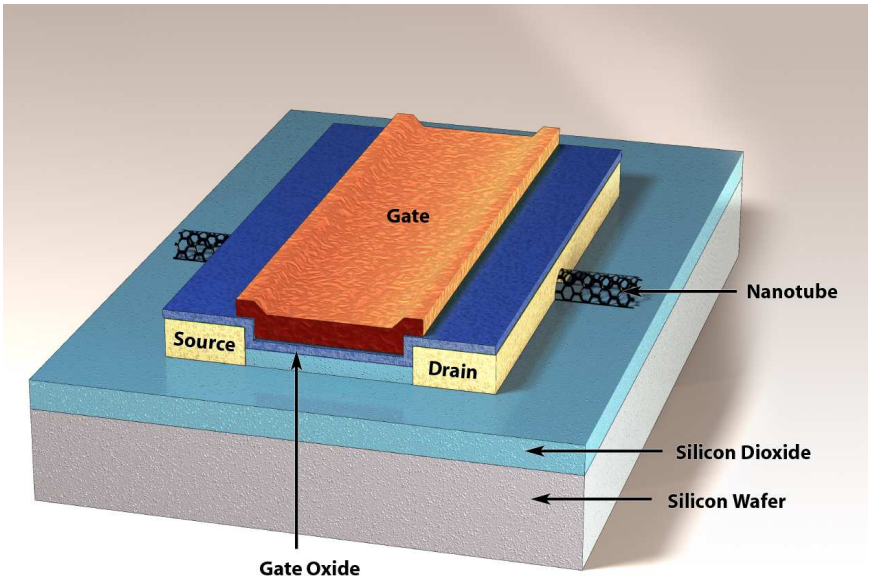


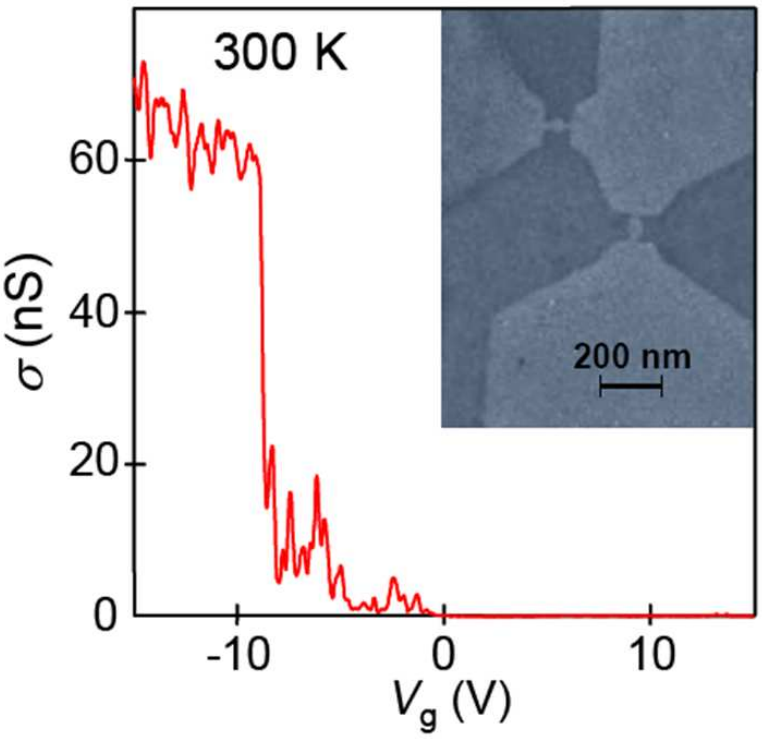
Figure 1.6: Single electron transistor inverter pattern on PMMA.

a form of carbon with unique transport and mechanical properties. Nanotubes can be metallic or semiconducting, and single wall or multi wall depending on their structure and fabrication processes. The main challenges of today's nanotube devices are the alignment and repeatability which limit their wide spread use. Despite their practical processing issues, carbon nanotubes can be implemented as transistor devices with extraordinary current carrying capability. Fig 1.7(a) shows the schematic of a carbon nanotube field effect transistor.

Recently, the basis of carbon nanotubes, 1D graphene layer has demonstrated electric field effect, initiated a growing amount of research into this field[37]. Graphene films can be prepared by means of exfoliation, or repeated peeling of high oriented pyrolytic graphite. Graphene based devices have been readily researched and implemented. The world's first graphene transistor was fabricated in 2007 (as shown in Fig 1.7(b)), opened a new page in the research of next generation transistors[3].



(a) Schematic of IBM's carbon nanotube field effect transistor (CNFET)[38].



(b) 10nm graphene quantum dot device with controllable conductance at 300K.

Figure 1.7: Carbon nanotube and graphene transistor devices, image taken from [3].

1.2.2.3 Nanowire transistors

Nanowires are other promising candidates that can be used as the building blocks for future transistor electronics. Silicon and germanium nanowire devices have been researched extensively for possible use in integrated nanoscale electronics[4]. Unlike a conventional CMOS device, a nanowire transistor utilises a thin nanowire as drain-and-source channel, with potential of more efficient switching and significantly reduced short channel effects. Figure 1.8 shows the schematic and cross section of a field effect nanowire transistor that utilises high-k dielectric material and a Ge/Si nanowire. The nanowire diameter of this device is around 15nm and can outperform a CMOS device by three or four times[5].

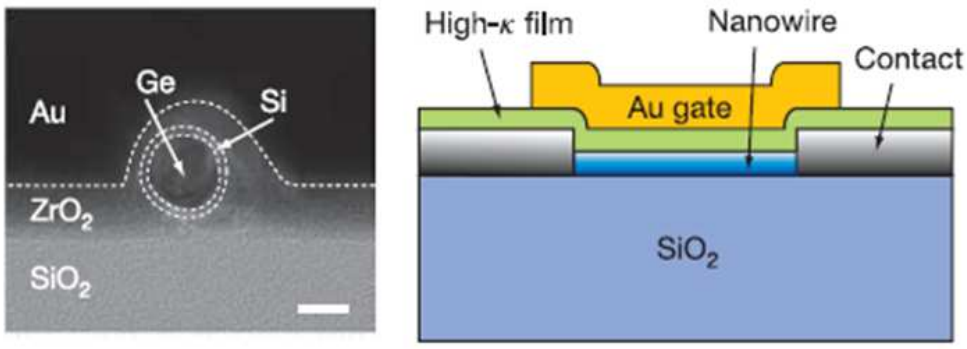


Figure 1.8: Ge/Si nanowire field effect transistor. Left: Cross section of the Ge/Si/ZrO2 heterostructure. Right: Schematic of the nanowire transistor device[4][5].

There is also growing interest in the research of semimetallic nanowire devices for transistor applications, such as bismuth nanowire which exhibits unique transport and field effect properties [9]. Similar to 1D graphene, the electric field effects of bismuth nanowire are of great interest, capable of achieving hole only or electron only carrier types in the nanowire[3][10]. The physical properties of bismuth will be further discussed in Chapter 5.

1.3 Project motivation and thesis layout

1.3.1 Project motivation

The advancement of current technology has allowed us to fabricate engineered structures into the nanoscale regime. However the fabrication processes involved in the pattern transfer and the integration into functional devices are often complicated. Nanowires play an important role in the development of next generation electronics such as interconnections for small scale devices, field emission arrays and sensor devices. Metallic and semimetallic nanowires, are especially interesting due to their high current density and high conductivity that are far superior than the semiconductor based devices. In 2004, Rotkin and Hess studied the idea of a field effect transistor device with a channel made from one metallic carbon nanotube[39]. However, the possibility of achieving electron depletion of metal nanowire with diameter close or smaller than the screening length has never been researched due to the difficulties of fabrication. The aim of this project is to develop a reliable and controllable approach for the fabrication, and characterisation of metallic and semimetallic nanowires with smallest possible dimensions. This is followed by implementing the nanowires into transistor structures with lateral gates for field effect studies. The physical geometry and the use of one type of material for the construction of these devices can allow the use of nanoimprint technology in terms of efficient and economical fabrication.

1.3.2 Thesis layout

This thesis details the fabrication and characterisation of metallic nanowire structures. The chapters in this thesis are arranged as follows:

- Chapter 1 described the introduction and motivation for the development of nano scale structures and devices.
- Chapter 2 covers main practical limits of current CMOS technology and the theory behind electric field penetration of metals, where the design of new nanowire devices and their operation principles are explained.

- Chapter 3 presents the technical details of the equipments employed in the fabrication and electrical characterisation.

- Chapter 4 details the design, fabrication and experiments for creating nanowire structures using EBL, where optimisations of fabrication parameters and challenging issues involved in the fabrication will be discussed. These experiments have allowed us to explore factors that limit the resolutions involved in the fabrication processes.

- Chapter 5 elaborates the development of fabrication process and experimental challenges for milling bismuth nanowire structures using focused ion beam milling (FIB) system, where approaches used for forming ohmic contacts to material with thick oxide coating are explored.

- Chapter 6 presents the electrical characterisation results for fabricated metallic and semimetallic nanostructures. Where the resistances and electric field effect measurements have been performed using semiconductor parameter analysers.

- Chapter 7 concludes the main findings of this thesis, and suggests the thoughts for the future works.

List of published works by the author is presented in Appendix A.

Chapter 2

Background and literature review

In the previous chapter, the fabrication limits for downscaling CMOS circuits have been discussed. As the scaling of planar CMOS transistors evolves, several practical limits that were once neglected in the scaling rule have now become the real limitations for transistor performance.

Rotkin[39] proposed the electric field effect for metallic nanotubes, with potential for metal transistors applications. As an alternative approach, we have explored metallic nanowire structures that consist of thin metallic nanowire channels and lateral gates. The use of metal nanowires as channels allows simpler fabrication steps, higher integration density, less short channel effects over semiconducting materials. This chapter covers some of the practical limits for CMOS scaling such as short channel effects (SCE), and high parasitic impedances. It is followed by the discussions of the possibility of metallic transistors, where the effect of electric field penetration into metals for thin metallic layers, and the design of metallic nanowire structures suitable for electric field effect study of various metals are presented.

2.1 Practical limits of CMOS

The downscaling of transistor features for higher density of integration has been successful as a strategy to improve performance. However, when the feature size of CMOS is small enough, practical limits like short channel effects, higher ratio of parasitic resistances and capacitances can no longer be neglected. In fact, these effects have recently been considered as the real limitations[6] to CMOS scaling as the technology advances to the 20nm node[40].

2.1.1 Short channel effects and tunneling

As the gate length is reduced to facilitate for the increase of integration density and operation speed, the so-called short-channel effects arise. Short channel effects can be realised from many aspects which not only impose a limitation of carrier transport in the channel but also affects the threshold voltage due to the reduced channel length[41]. One type of the short channel effect is called the punchthrough effect, as illustrated in Figure 2.1. It arises when the channel length is short enough that the depletion layers of the two junctions merge together, resulting in undesired transistor operation. Moreover, due to the short length of channel, the barrier height at the source will be lowered by the drain voltage, leading to large sub-threshold current. This effect is called drain induced barrier lowering (DIBL)[42], and it has immediate impact on power dissipation of CMOS transistors. Although some of these short channel effects can be improved by means of employing thinner oxides, multigate structures[43], higher substrate doping, shallower extensions of junctions[35], metal gates and high-k dielectric materials[44], they have indeed set a hard limit on the smallest achievable size for current planar CMOS devices.

Another practical limit for nanoscale CMOS transistor is tunneling. According to the scaling rule set by Dennard[22], the thickness of a gate oxide has to be scaled according to its lateral size to account for short channel effects. At 90nm technology node, the thickness of gate oxide is set to be 1.2nm, equivalent to only 5 atomic layers thick of oxide. This thin dielectric allows direct tunneling from gate into the film, resulting in a high gate leakage current. Al-

though the state of art CMOS transistors today utilise high-k dielectric materials and metal gates to overcome the gate leakage and scaling problems, gate to dielectric tunneling can still be one of the major obstacles to the next generation transistors. Figure 2.2 shows the two types of tunneling effects often found in a conventional CMOS device, the gate to dielectric tunneling and source to drain tunneling. Generally speaking, direct drain-source tunneling will be more likely to occur for devices with sub 10nm long channels[45][46].

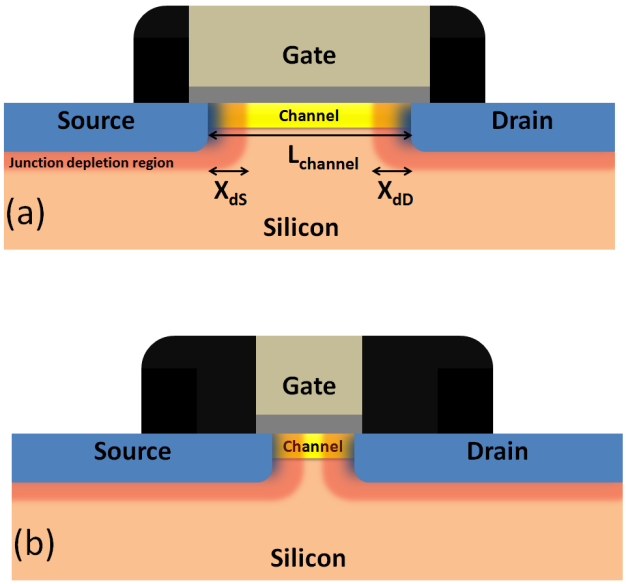


Figure 2.1: Punch through effect in short channel semiconductor transistor. (a)Channel length is larger than the junction depletion widths. (b)Channel length is comparable to the junction depletion layers, resulting in undesired punchthrough effect.

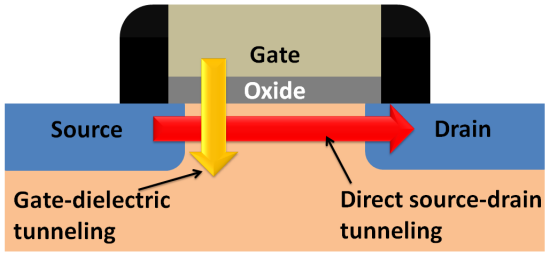


Figure 2.2: Two types of tunneling effects in planar CMOS: gate-dielectric and source drain tunneling.

2.1.2 The rise of parasitic resistance and capacitance

Today's CMOS transistors are integrated in a high density manner that the distance between each neighbouring devices has decreased to tens of nanometers. The contacts, at the meantime, have to be scaled to account for the reduction in device spacing and gate lengths, resulting in increased parasitic resistances and contact to gate capacitances[47]. Figure 2.3 shows a typical design rule model and the corresponding parasitic resistance and capacitance components of planar Si transistors for the 32nm technology node[6]. In this technology, the transistors have 100nm pitch with drain to gate contact spacings of 25nm.

The scaling of contact sizes and device spacing has reflected the abrupt increase in the parasitic impedances within the past few decades[48]. It will soon become comparable to the channel resistance as the technology advances. Figure 2.4 illustrate the impact of the parasitics to the IC industries when the channel resistances and capacitances become comparable to parasitic components[6]. These parasitic components have indeed been considered as the real limitations for future CMOS scaling and have a direct impact on further improvement of performance and operation in the near future.

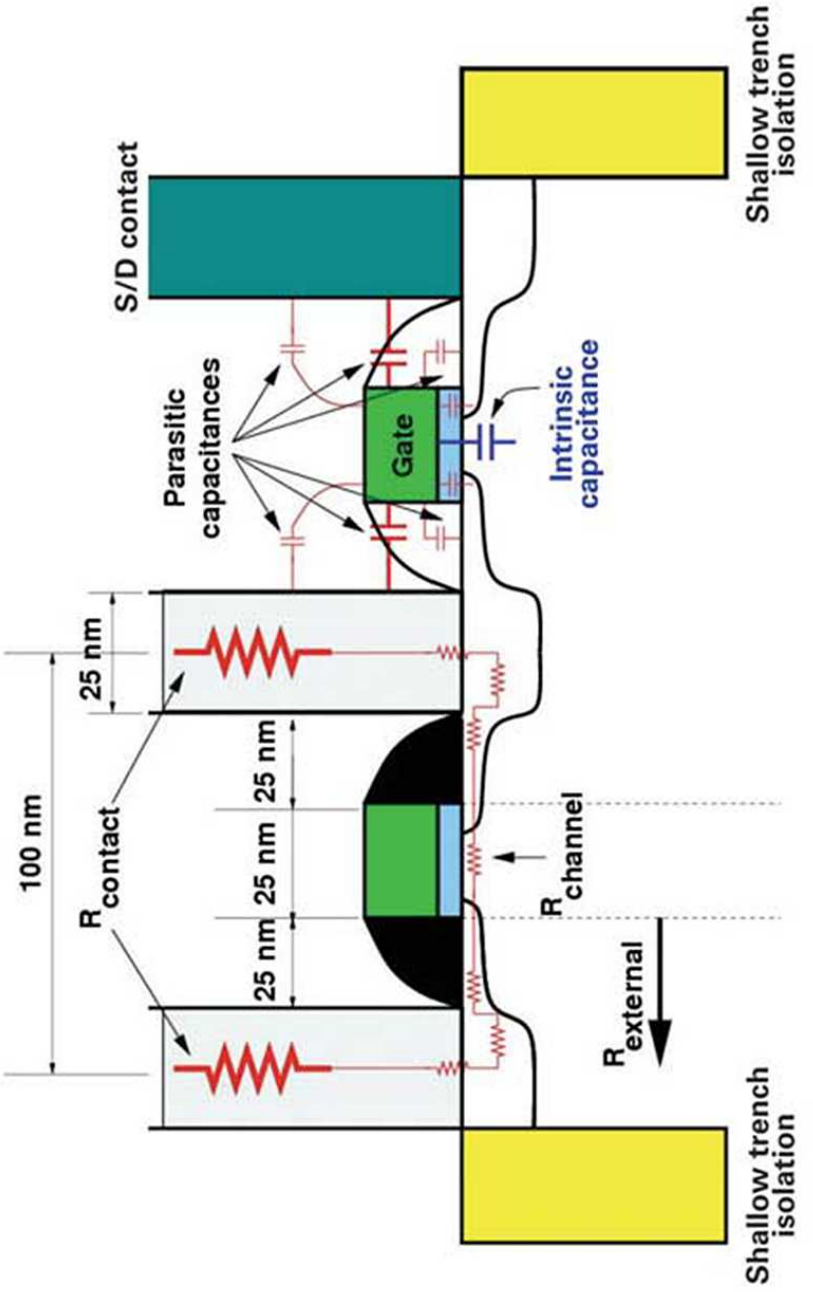
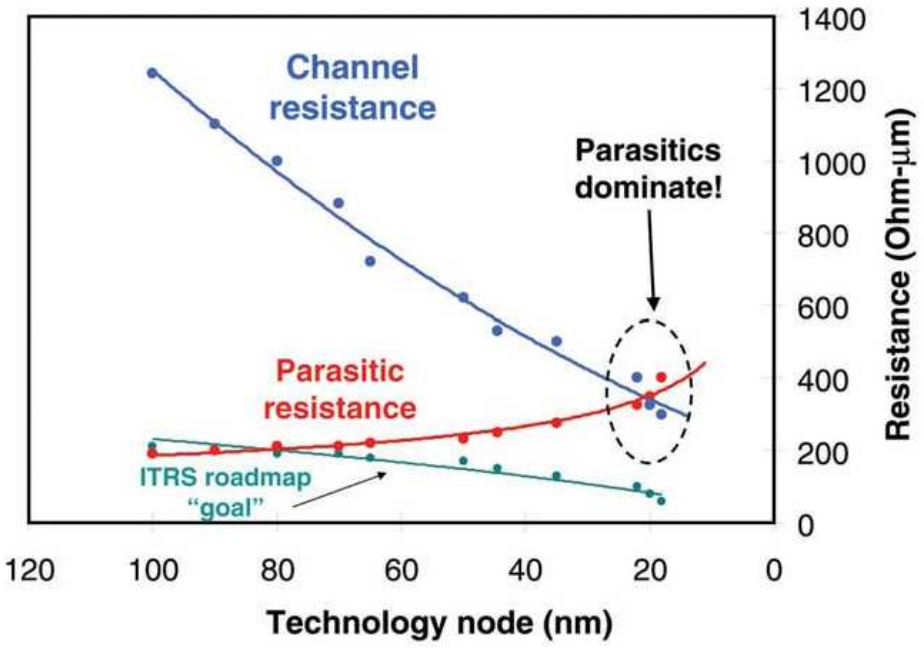
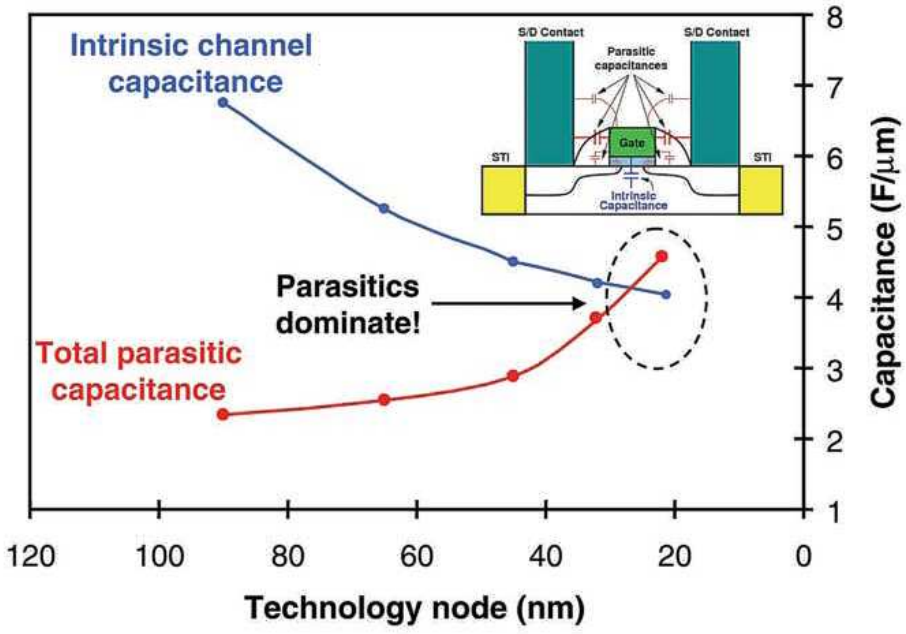


Figure 2.3: Planar CMOS structure with various parasitic resistances and capacitances, adopted from [6].



(a) Total parasitic and channel resistances versus technology nodes.



(b) Total parasitic and channel capacitances versus technology nodes.

Figure 2.4: The rise of parasitic resistances and capacitances with down sizing of transistors, adopted from [6].

2.2 Possibility of metallic transistors

While the current fabrication towards 32nm node and beyond have proven to be extremely challenging and high cost, the quantum effects for ultra short channel CMOS have limited the performance and power dissipation, signaling to the industry the end of Moore's law is near. As the requirement for the investigations of new types of materials and structures for the next generation transistor devices, we have explored the idea of an all metal double lateral gate nanotransistor structure which utilises one thin metallic nanowire as drain and source channel for the higher transconductance and improved short channel effects over silicon transistors.

The high conductivity of the metal channel eliminates the practical limit of punchthrough effect even for a channel of just few nanometers long, it also allows the contacts to be integrated in higher density comparing to conventional metal silicate contacts used in CMOS transistor. In addition, the one dimensional nature of metallic nanotransistor allows the device to be replicated using nanoimprint technology, suitable for a wide variety of substrates.

Generally speaking, metallic nanotransistors should outperform conventional Si transistors in terms of performance, integration density, parasitic resistances, and fabrication costs due to the significantly higher conductivities, less short channel restrictions and single step lithography process. However, a metallic nanotransistor requires an ultra thin nanowire channel, comparable to the screening depth and the electric field penetration of metals to allow acceptable transistor operations. This has created great challenges for the fabrication as the required dimensions for metallic nanowires are just few nanometers in diameter[49][50].

2.2.1 Electric field penetration into metal

Unlike a semiconductor, the conduction band in a conductor partially overlaps the valence band, allowing valence electrons to participate in conduction freely. Consequently the conductivity of a conductor is much greater than that of a intrinsic semiconductor[51]. Metals belong to conductors that are known to

exhibit strong damping of external electric fields screened by the large number of charge carriers, where the screening depth is the measure of the field penetration[52] into the material. The strong screening in metals can result in extremely small electric field penetration depths that are normally neglected. However, when it comes to nanoscale metallic nanowire with diameter comparable to a few nanometers, the field penetration could induce depletion or accumulation of electrons in metal, with potential of achieving a gate effect suitable for transistor operation.

The effect of static electric field penetration into metals was first studied by Rice in 1928, where degenerate Fermi statistics was used to show that the diffused space charge layer acted like a constant capacitance for mercury electrodes separated by a fraction of an angstrom by vacuum[53]. This effect has been revisited and approximated by few groups using other approaches such as solving the Hartree fock equation for the free electron model[54], solving the Schrödinger equations[55], and finally, a much simpler model, with the use of Thomas Fermi approximation[56] for the realisation of an exponentially decayed electric field inside the conductor[7].

Figure 2.5 shows the schematic for metal and dielectric junctions in a thin film capacitor, where in most cases the displacement charge in the electrodes were assumed to exist at the electrode and dielectric interface (Figure 2.5(b)). A more realistic model can be depicted as in Figure 2.5(c), where the electric field is assumed to decay exponentially from the surface ($x = 0$) of the conductor until a finite spatial extent of distance L.

Black[7] has modeled this electric field damping using a simple exponential function in terms of induced charge density function. By looking at the right hand electrode in Figure 2.5:

$$\rho(x) = \rho_{max} e^{-\frac{x}{L}} \tag{2.1}$$

where ρ is the surface charge density at the metal/dielectric interface, and L characterises the distribution of charge over a finite distance within the electrode. The electric displacement in the metal can be fitted into the Gauss law at which:

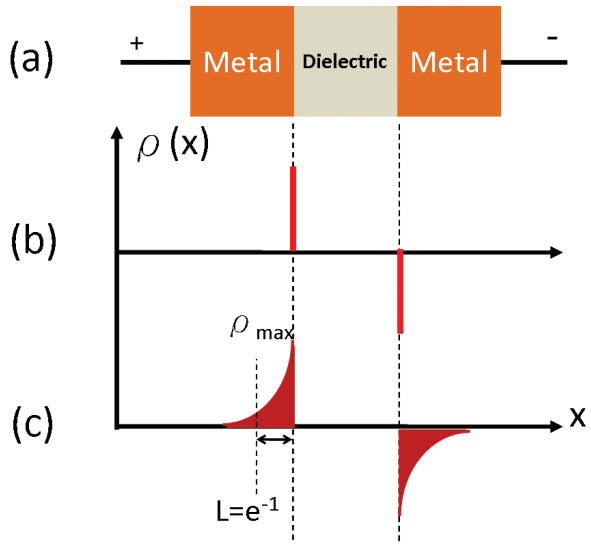


Figure 2.5: (a)The simple schematic of metal-dielectric junctions. (b)Displacement charge distribution in the simplest approximation. (c)A more realistic model that consists of displacement charge over a finite extent[7].

$$\nabla \cdot D(x) = \rho(x) \tag{2.2}$$

From Equation 2.2, the total displacement charge per unit area is therefore:

$$D_{total} = \int \rho(x)dx = \rho_{max}L \tag{2.3}$$

2.2.2 Thomas fermi approximation

In this approach, we used the Thomas-Fermi model for approximating the effective screen length L for an exponentially damped electric field within metals. This can be utilised to evaluate the potential and electron density of any point within an electron gas[56]. The Thomas-Fermi approximation relates the local chemical potential at one point to the electron concentration in an electron gas cloud at the same point, where the induced charge density $\rho_{ind}(x)$ can be approximated by[57]:

$$\rho_{ind}(x) = -e\frac{3\rho_0}{2}\frac{\Phi(x)}{E_F} \tag{2.4}$$

where e is electron charge, ρ_0 is the bulk charge density of metal surface and $\phi(x)$ and E_F are the electrostatic potential and Fermi energy of the metal

respectively.

Based on Black's model[7] we can relate the electric potential for point within the surface of metal to a point much deeper in the metal $\rho(x)$ by:

$$\Phi(x) = -E \int ds = -\int \frac{D(x)}{\varepsilon_0 \varepsilon_m} dx \tag{2.5}$$

The screening depth for metal is finite and we can assume that the field deep within the electrode to be 0, which yields the simple model approximation for the electrostatic potential to the induced charge density.

$$-\int \int \frac{\rho(x)}{\varepsilon_0 \varepsilon_m} dx = \left[-\frac{L^2 \rho(x)}{\varepsilon_0 \varepsilon_m} \right]_x^{deep} = \frac{L^2 \rho(x)}{\varepsilon_0 \varepsilon_m} \tag{2.6}$$

The surface potential at the metal-dielectric interface is therefore:

$$\phi(0) = \frac{\rho_{max} L^2}{\varepsilon_0 \varepsilon_m} = \frac{D_{total} L}{\varepsilon_0 \varepsilon_m} \tag{2.7}$$

From Equation 2.5 to 2.7, the effective dielectric constant, ε_m is incorporated to describe the polarisibility for electrons bound to ionic cores*. Previous studies have measured the effective dielectric constant for the bound electrons for Ag and Cu to be ε_m 2.5 and ε_m 4.8, deduced by applying Kramers-Kronig relations to reflectance data obtained near normal incidence[58].

The field penetration length, L, can now be solved by substituting Equation 2.7 into the Thomas Fermi approximation result in Equation 2.4, which yields:

$$\rho_{ind}(x = 0) = \rho_{max} \cong -e\rho_0 \frac{3\rho_{max} L^2}{2\varepsilon_0 \varepsilon_m E_F} \tag{2.8}$$

Hence, the field penetration distance, L, into the metal can be expressed in terms of the Thomas Fermi approximation model for an exponentially decayed field as the following. The term $\frac{2}{3}\frac{\varepsilon_0 E_F}{\rho_0 e}$ is normally expressed as ℓ_{TF}^2, where ℓ_{TF} is commonly known as the Thomas Fermi screening length[59] in bulk material.

$$L^2 = \varepsilon_m \frac{2}{3} \frac{\varepsilon_0 E_F}{\rho_0 e} \tag{2.9}$$

*Bulk Metals are often assumed to have an enormous static dielectric constant; in the case for electric field penetration within metal layers, the bound electrons are also responsible for screening, and the polarisation response for the underlying lattice ions will be finite[7].

Strictly speaking, this approximation based on the Thomas Fermi model can only be used to represent the screening for a relatively small electric field, that is, $e\Phi(x) < E_F$, under static condition and low temperature[7][57]. At this stage, we can extract the field penetration term based on a relatively small field. This model indicates a relationship between expected screening depth to the effective dielectric constant, Fermi energy and bulk conduction electron density in a metal. Based on the formula, $L^2 = \varepsilon_m \frac{2}{3} \frac{\varepsilon_0 E_F}{\rho_0 e}$, we can calculate the field penetration depth, L, in terms of the intrinsic property of the metal. The screening depth could be increased by means of increased Fermi energy level, reduced electron density[†] For Ag ($\varepsilon_m = 2.5$) and Cu ($\varepsilon_m = 4.8$) to be $0.93\mathring{A}$[‡] and $1.23\mathring{A}$ respectively[58]. A more sophisticated model is required to accommodate for a much larger electric field and in a dynamic environment, which is beyond the scope of this work.

[†]Fermi energy for a metal has a $n^{\frac{2}{3}}$ to the charge carrier concentration n.

[‡]This can be calculated using $E_F = 5.4$, and $\rho_0 = 5.86 \times 10^{28} C/cm^3$.

2.3 The design of metallic transistor structures

2.3.1 Operation principles

Rotkin[39] has proposed and discussed the possibility of electric field effects on 0.7nm and 1.4nm metallic single wall nanotube (M-SWNT). Since then, a number of studies and experiments have been carried out to research metallic nanotube transistors[60][61][62]. It has inspired us to explore and study planar metallic nanowire structures that are much easier to be fabricated and integrated into transistors.

In this work, we have developed the structure for a planar, nanoscale metallic transistor with potential for gate effect operation, where the device can be fabricated in a systematic and more controllable way. This type of transistor operates similarly to a JFET, by governing the flow of current through an ultra thin metallic nanowire channel. The use of metal as conduction channel eliminates the short channel effects as in conventional CMOS transistor, and at the same time, offer better integration density and transconductance properties. Figure 2.6 illustrates the operation principle for a electrostatic metallic nanotransistor. Considering a conduction channel made of few atoms wide metal nanowire, the quantum current is likely to flow unimpeded with applied drain and source bias. However, in the presence of an external electrostatic field that is sufficient to repel the flow of electrons and effectively penetrate into the nanowire, on the assumption that electron depletion around the surface and bound electrons will be induced, resulting in an abrupt decrease of conductance and hence switch off the transistor.

Another model is created based on the design of Y-branch semiconductor transistor proposed by Wesström in 1999[63]. In the Y-branch switch design, there are two drains branching from the source, and two lateral gates beside each of the drains, as shown in Figure 2.7. Without any external field from the gate electrodes, the current will flow evenly into both drains, as in Figure 2.7(a). The switching effect of the transistor can be done by what is known as the push pull operation. In this operation mode, one side gate will have a positive voltage applied whereas the other gate has a negative voltage applied. The positive

field will encourage current flow, and the negative field will discourage it. This yields a diversion of current into one of its branches, as shown in Figure 2.7(b). The Y-branch design can also be used in amplifying mode. By steering electrons down either drain, the voltage difference between the inputs is amplified, which results in a larger voltage difference between the branches.

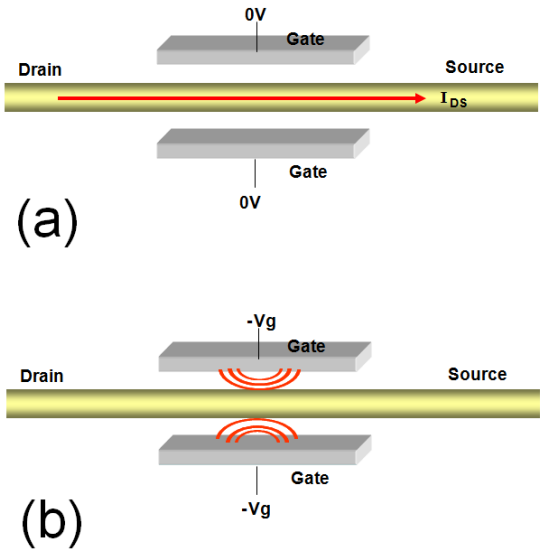


Figure 2.6: The operation principle for electrostatic metallic nanowire transistor, where the flow of current is controlled by the applied gate voltage:(a)Without external gate voltages (b)With applied electric field $-V_g$.

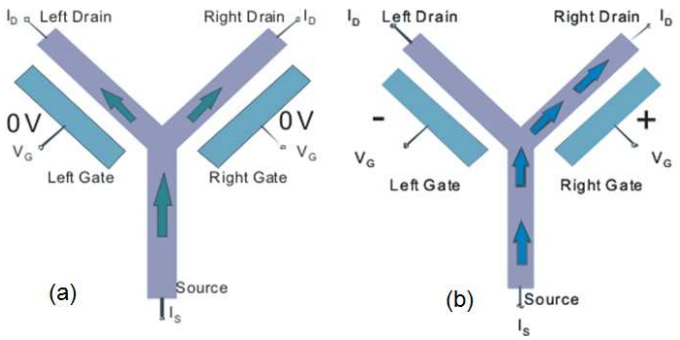


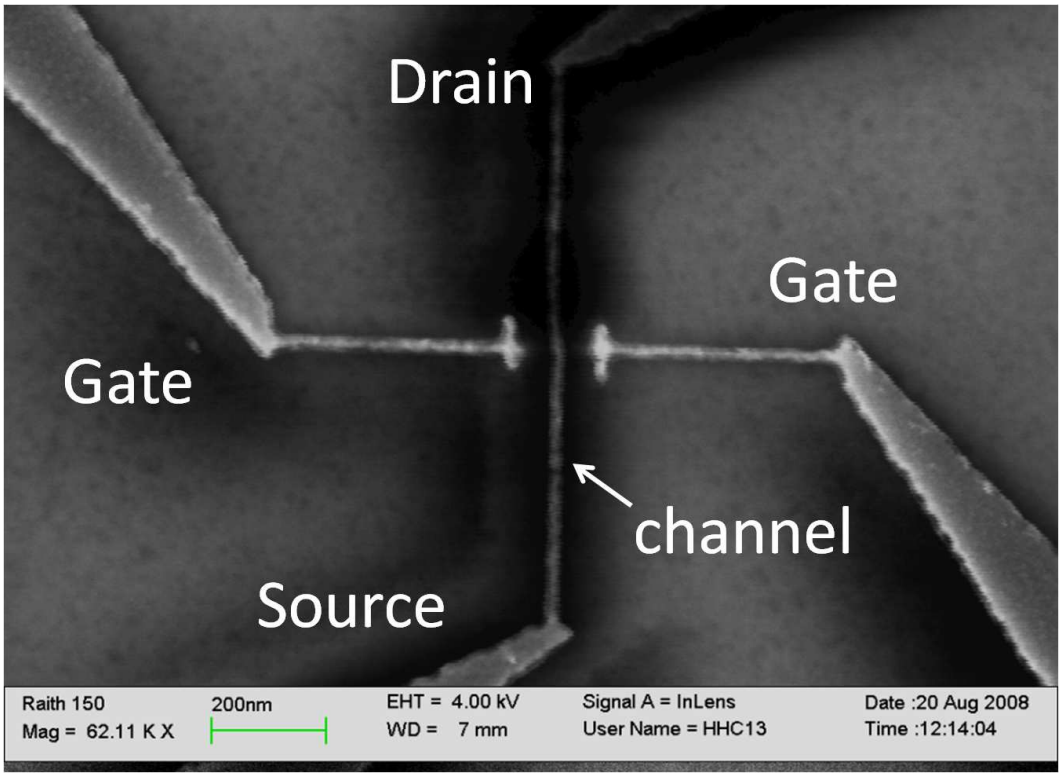
Figure 2.7: The operation principle for metallic Y-branch transistor, where the flow of current is controlled by the applied gate voltage:(a)Without external gate voltages (b)With applied electric field $-V_g$.

2.3.2 Device design and materials

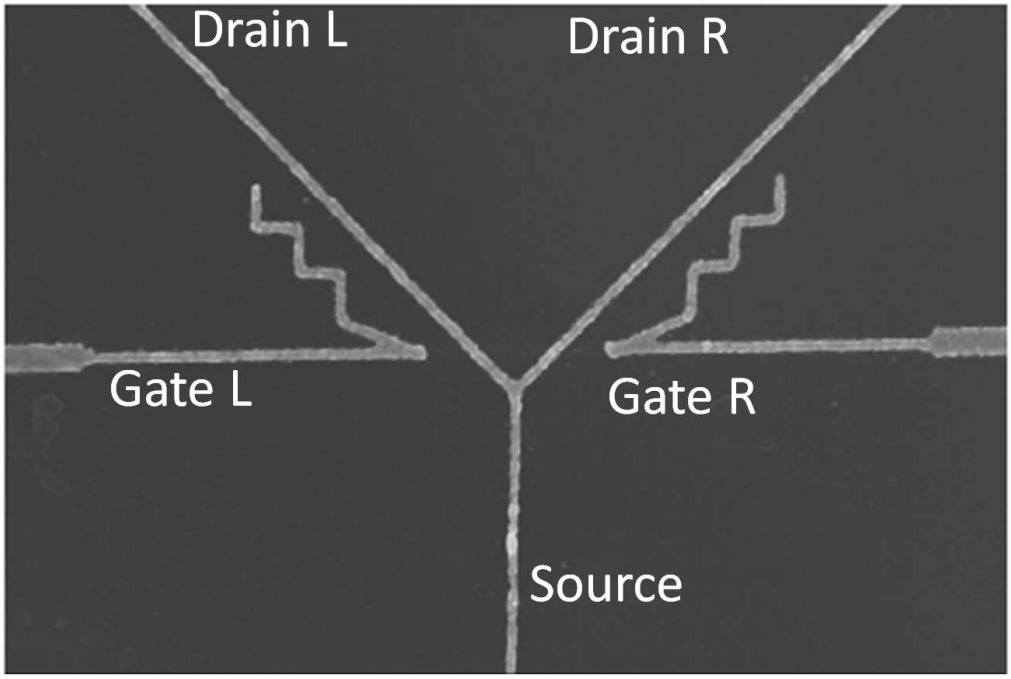
The nanowire dimensions for an ideal metallic transistor device are preferably a few nanometers in width for more effective functionality. While for metals with higher effective dielectric constant (ε_m), materials in the form of metal silicides, or metals that exhibit weak screening (e.g Bismuth), the nanowire can be made larger in diameter for device operation. The external electric field for this type of transistor can be applied by means of using gates in various geometries such as top/bottom gates as in Si CMOS[35], surrounding gates[64] or lateral gates[65] placed on the same plane as the nanowire. In this work, lateral gates were studied as we intended to develop a simpler fabrication process, compatible for nanoimprint technology for replication.

A number of structures have been designed which are suitable for characterising electric field penetration effects and electrical properties for nanowires. Figure 2.8(a) shows the basic components for metal nanotransistors, where the gates of the nanowire were designed to be 20nm-200nm away from the main nanowire, separated by air gaps. On the other hand, the widths and thicknesses of the nanowire, which decide effectiveness of electric field penetration, were made in the range of 12-200nm using the highest resolution patterning and deposition apparatuses available. In addition, Y-branch nanowire transistor structures, with the potential of diverting the current into one of the branches have also been designed and fabricated in this work as shown in Figure 2.8(b).

Electron beam lithography was employed to pattern sub 20nm features on resist, followed by the metallisation of the material suitable for both fabrication process and electrical characterisation. Ideally, the metal used in forming the channel should have the highest mobility and lowest electron concentration for enhancing the possibility of depletion and performance. We have successfully fabricated nanowire devices for transistor like structures using transition metals like Ag, Al, metal alloys like $Au_{0.6}Pd_{0.4}$, $Ni_{0.8}Cr_{0.2}$, and semimetal such as Bi. The details of fabrication of these devices are in Chapter 4 and Chapter 5 for metallic and semimetallic structures. Their electrical characterisation results can be found in Chapter 6.



(a) SEM image showing NiCr nanowire (12.5nm diameter) transistor structure with double lateral gates.



(b) SEM image showing Ag Y-branch (35nm diameter) transistor structure with two lateral gates.

Figure 2.8: The designed structures of metallic nanowires for electric field effect studies, the SEM images were taken normal to the surface of the devices.

2.4 Nanoimprint replication

Due to the planar structure and single material nature of metallic nanowire structures developed in this work, nanoimprint can be utilised as one step pattern transfer technology. Compared to the high cost and complicated fabrications for current Si transistors, metallic nanowire based structures with potential for nanotransistors in conjunction with nanoimprint patterning allow for a rapid and economic fabrication process that can be utilised for a wide range of substrates[28]. The nanoimprint mold is designed to be fabricated on transparent quartz substrate, and metallised with $Ni_{0.8}Cr_{0.2}$, followed by reactive ion etching (RIE) process. Figure 2.9 shows the standard UV-assisted nanoimprint process suitable for mass fabrication of metallic nanowires and nanotransistor structures.

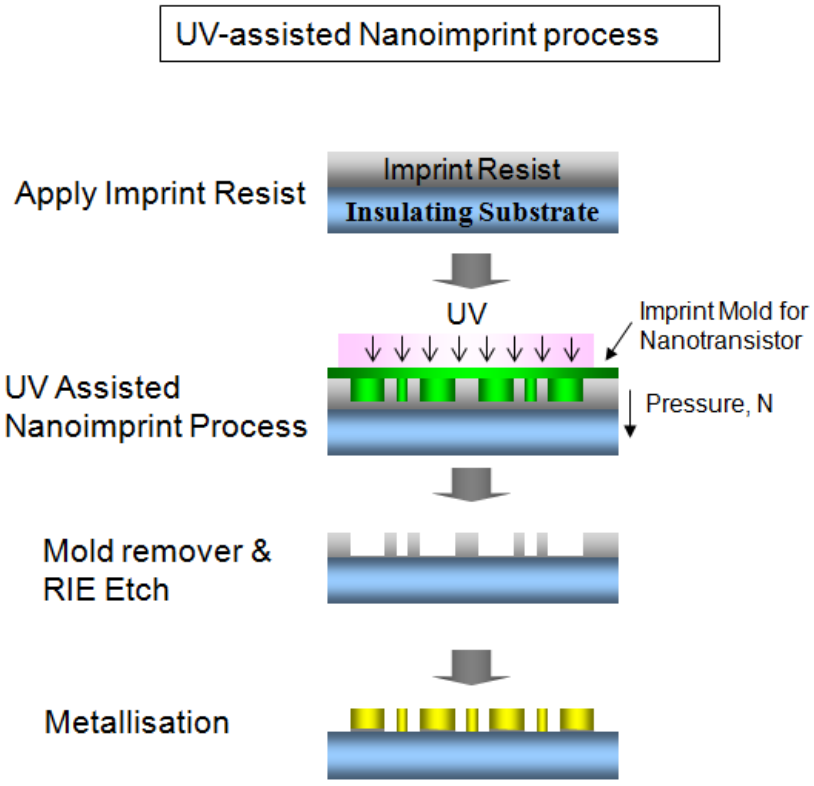


Figure 2.9: Nanoimprint process for replication of metallic transistor structures.

Chapter 3

Device fabrication technologies

In the development of the metallic nanowire based transistors, various nano and microelectronic fabrication and characterisation technologies were employed. These include the material deposition processes utilised to form high quality metal structures on the substrate, and the lithography processes used to define contact and nanowire features on resists. For the electrical characterisations of fabricated nanostructures, a number of resistance measurement techniques were performed in the semiconductor parameter analysers, including two point and four point resistance measurement, transmission line measurement, and Gate effect measurement. This chapter gives a brief overview of processing and characterisation technologies utilised to fabricate and study metallic and semimetallic nanowire structures.

3.1 Material deposition

In the fabrication of metallic nanowire based transistor structures, materials used as nanowire channel, electrical contacts, and dielectric layers were deposited using thermal, electron beam evaporation and magnetron sputtering techniques. The parameter for each of the deposition tools have been optimised experimentally to provide high quality and continuous film required for successful device operations.

Although evaporation is still widely used in research for metal deposition, it is now being frequently replaced by sputtering technology in the industry due to the step coverage issues. Figure 3.1 shows a simple scheme where step coverage takes part in depositing materials on a feature with aspect ratio of 1. The evaporated films are likely to become discontinuous and break off around the vertical side walls of the resist (Figure 3.1(a)). Although a poor step coverage of surface topology can be considered as one limiting factor of evaporation, lift-off can benefit from this factor and can be utilised to process materials that are difficult to etch [25]. In order to deposit materials for the fabrication of nanowire devices, these deposition technologies have been studied in depth. Among the deposition apparatuses available in the nanofabrication lab at the University of Canterbury, thermal evaporation has been used mainly for metal depositions on E-beam patterned samples. RF sputtering was employed for Ag thin film and dielectric deposition. The electron beam evaporation, on the other hand, was found to cause substrate damage and electron sensitive resist deformation, leading to unsuccessful lift-offs.

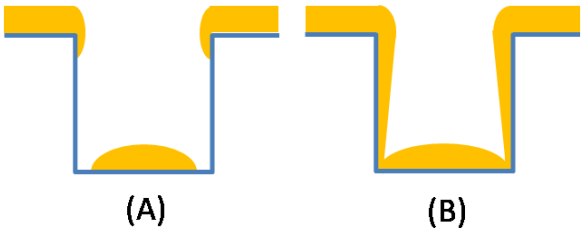


Figure 3.1: Step coverage in physical deposition methods: (A)Thermal evaporation (B)Sputtering (heated and rotated).

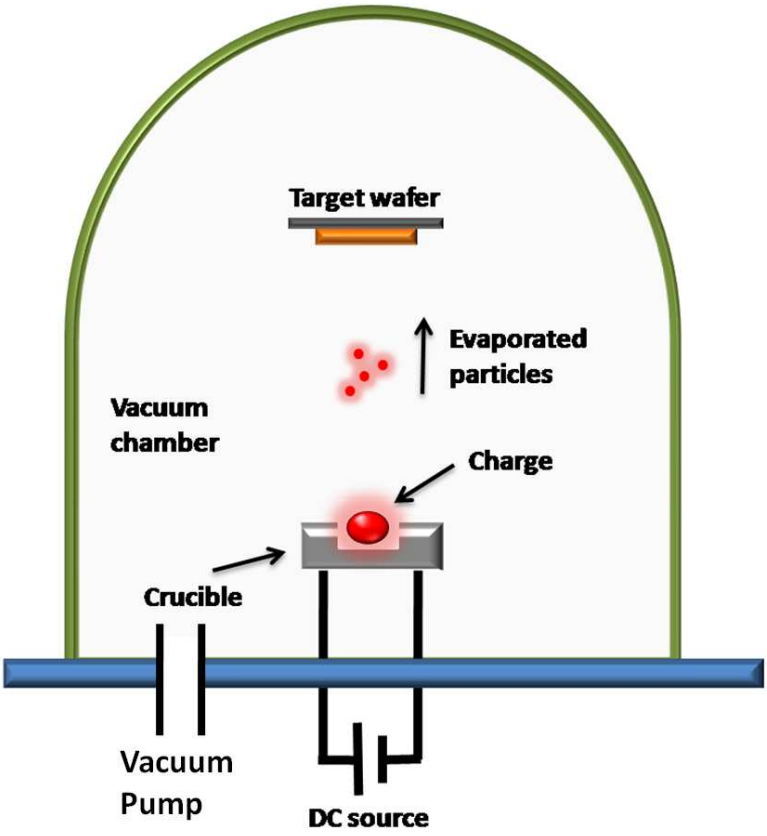
3.1.1 Thermal evaporation

Thermal evaporation can be considered as one of the most commonly used metal deposition technique. Prior to the evaporation process, the vacuum chamber is first pumped to the optimal evaporation base pressure, where the target deposition material, often called charge, is heated in a crucible through a resistive media. As the charge has been heated to sufficiently high temperature, it will start giving off vapor that recondenses and forms a thin film onto the surface of a sample mounted near the top of the chamber. The thickness of deposited film is normally monitored in-situ by a quartz crystal oscillator positioned near the wafer. These thickness values are computed by the crystal monitor system based on the variation of oscillating frequency of quartz crystal, the density of deposited material, the acoustic impendence, and the tooling factor of evaporator system. In order to deposit materials to the wafer in a most straight line path, vacuum level as low as 10^{-5} torr is often desired, which can be deduced from the mean free path of air using the formula:

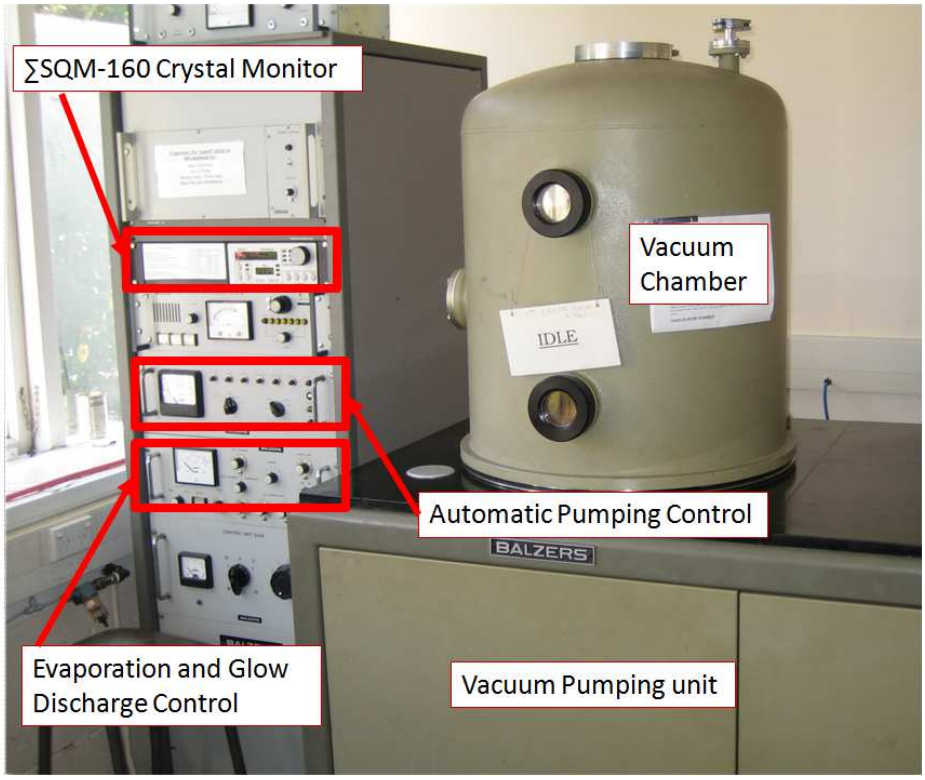
$$\lambda_{mfp} = \frac{5 \times 10^{-3}}{P} \tag{3.1}$$

where the mean free path of air, λ is in centimeter and the pressure, P is in unit of Torr. At 10^{-5} Torr, the mean free path of air at 25°C is approximately 50cm. It can be considered as a good indicator for the minimum vertical distance required between crucible and substrate wafer for good quality deposition in a chamber[66].

In this work, a Balzer 510A thermal evaporator was employed in the depositions of metals for electrical contacts, and metallic nanowire structures. Figure 3.2 shows the schematic of the key internal components of a common thermal evaporator. Balzers 510A evaporator is equipped with a diffusion pump capable of delivering a base pressure of down to the 10^{-7}torr range to the system, and the charge, situated near the bottom of the bell jar vacuum, is heated by supplying a high current through the molybdenum aluminium oxide ($MoAl_2O_3$) boat of the crucible. In addition, this system allows multisource sequential evaporation, where up to two different materials can be deposited onto the target without breaking the vacuum.



(a) A simple schematic of thermal evaporation.



(b) Balzers 510A thermal evaporator.

Figure 3.2: Thermal evaporation process and the apparatus used in this study.

In terms of deposition film thickness monitoring, $\sum$ SQM-160 crystal monitoring system was used. The tooling factors for evaporating various materials in this system have been experimentally determined*. Table 3.1 lists the evaporation parameters of materials used in this study [67].

Table 3.1: List of thermal evaporation parameters for materials used, where Z stands for acoustic impedances of materials.

Materials	Density(g/cm^3)	Z	†Power	Tooling	Rate ($\AA$/s)
Au	19.30	23.18	4.5	1.0	10-15
Ag	10.50	4.67	4	1.1	15-30
NiCr	8.50	8.83	5.25	0.9	1-3
Al	2.70	8.20	3.75	1.0	10-15
Ti	4.50	14.06	5	1.0	5-9
Bi	9.80	11.18	*81A	1.0	1

3.1.2 DC and RF Sputtering

Sputtering has been commonly used for the deposition of metal, alloys, and dielectric materials and it is the primary alternative for the replacement of evaporation technology in industry. Among the deposition processes, sputtering offers better step coverage than evaporation, less substrate and resist damage than e-beam evaporation, and more importantly, capable of depositing a broad range of materials. Fig 3.3(b) shows the Edwards Auto-500 magnetron sputtering system in the University of Canterbury, it is equipped with direct current (DC), radio frequency (RF) sputtering magnetron sources and an electron beam evaporation attachment. Figure 3.3(a) shows the basic operation principle of a DC sputtering process.

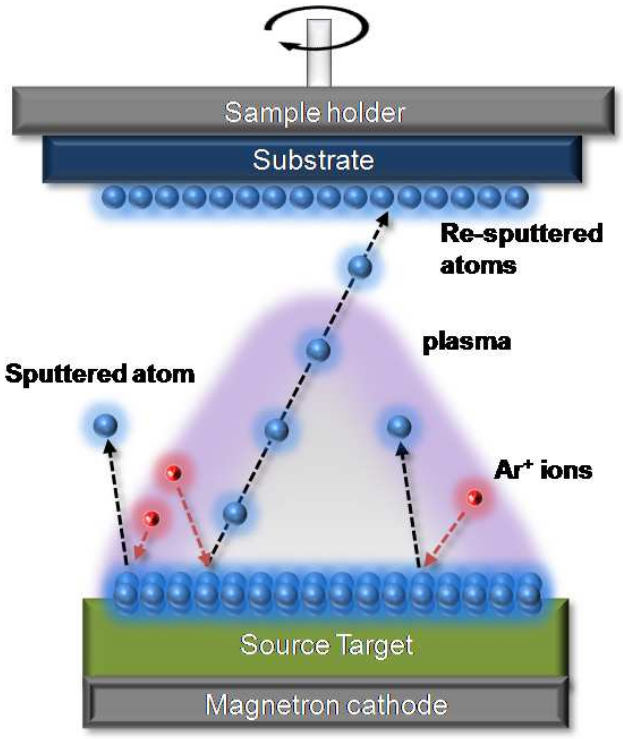
*The thickness of thin films were measured using Veeco DEKTAK150.

†The power setting factors are experimentally determined in a Balzers 510A system. For Bi evaporation, a dedicated evaporator was employed at the National Cheng Kung University, Taiwan, where the power setting was controlled by entering the current in amperes.

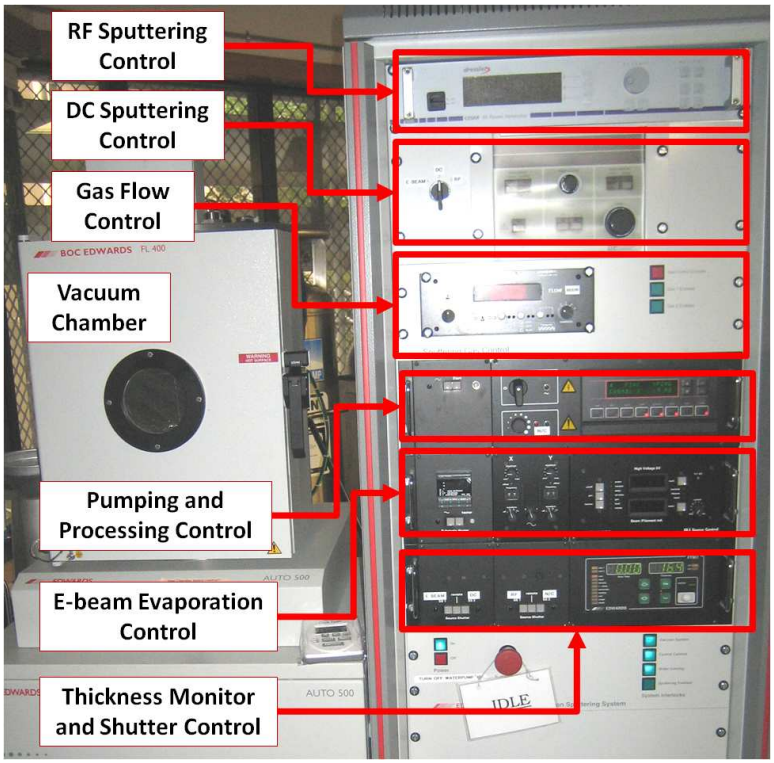
During the DC sputtering process, inert gas such as Argon is introduced and forms a plasma, where this plasma will be confined above the source target by a magnetic field. As the energetic ions of the plasma bombarded the surface of the source target, atoms of target materials are knocked off from the surface and transported into the vacuum chamber in random directions. These atoms are then re-sputtered and deposited onto the substrate placed above the plasma and source target. In order to achieve good uniformity and step coverage of the deposition, the substrate is often rotated and heated.

DC and RF sputtering are two common modes for depositing metal and semicoducting/dielectric materials in a sputterer. The main difference of these two modes is the applied potential to the source target. For RF sputtering, a RF power between 25W to 200W at 13.56MHz is used. This prevents poorer conductive source target materials such as semiconductors and dielectrics to heat up and crack due to thermal expansion.

In this study, DC sputtering was mainly used in depositing tungsten as an anti-charging layer for imprint mold making. Tungsten has a high melting temperature at 3422°C and is not ideal to be deposited using thermal evaporation [68], whereas it can be easily deposited on quartz substrate with good uniformity using a DC sputtering process. On the other hand, RF sputtering has been used for the deposition of SiO_2 and high quality Ag thin films for gate dielectrics and transistor channels.



(a) DC sputtering operation principle.



(b) Edwards Auto-500 Magnetron sputtering system.

Figure 3.3: The operation principle and key components of the Edwards Auto-500 magnetron sputtering system.

3.1.3 Electron beam evaporation

The Edwards-500 sputtering system is equipped with an 5KeV electron beam (E-beam) evaporation unit. Unlike thermal evaporation, in an electron beam evaporation process, the charge in the crucible is heated by a flux of electron beam bent by a strong magnetic field. The high energy electron beam in most E-beam evaporation systems is emitted from a tungsten filament [69]. This flux of electron beam creates a localised heating on the crucible unit, where only the charge is scanned and heated while the crucible is cooled to avoid cross-contaminations. Figure 3.4 shows the schematic of a common electron beam evaporation system.

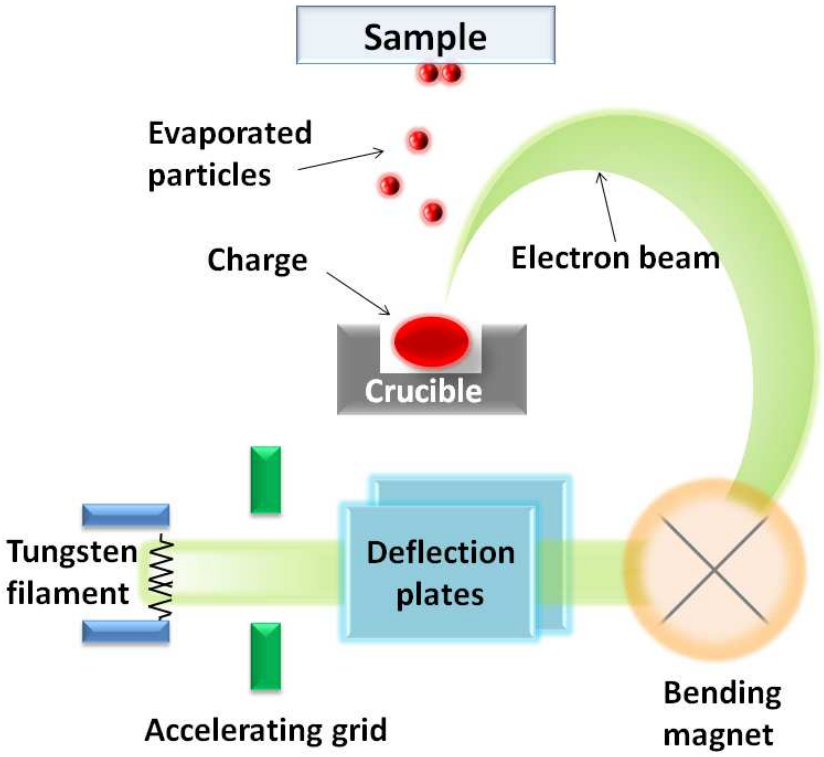


Figure 3.4: A simple schematic illustrating key components in an electron beam evaporation system.

Although E-beam evaporation can be used to deposit a wide range of materials, there exists two major limiting factors. These are radiation damage and non-uniform coating for thermal insulating and soft materials like SiO_2 and silver [70][71], where RF sputtering can usually yield higher quality thin films. Electron beam evaporation in this work has been employed mainly for the deposi-

tion of AuPd used for gate electrodes for Ag thin film devices and Al nanowires respectively. Table 3.2 shows the sputtering and electron beam deposition parameters for the deposition of materials using Edwards 500 magnetron system in this research.

Table 3.2: List of DC and RF sputtering and E-beam evaporation (EB) parameters for materials used in this study, where D and Z stand for density (g/cm^3) and acoustic impedances of materials.

Materials	Mode	Gas	D	Z	Power	Tooling	Rate (nm/min)
Ag	RF	10Ar	10.50	4.67	50W	1.5	7.5
Ag	EB		10.50	4.67	45mA	1.4	1
W	DC	Ar	19.30	54.17	300W	1.2	15
Al	EB		2.70	8.20	35mA	1.5	1.5
Pt	EB		21.40	36.04	200mA	1.0	6
AuPd	EB		16.39	2.4	140mA	1.0	5
SiO_2	RF	10Ar	2.13	10.15	200W	8.0	1.5

3.2 Processing technologies

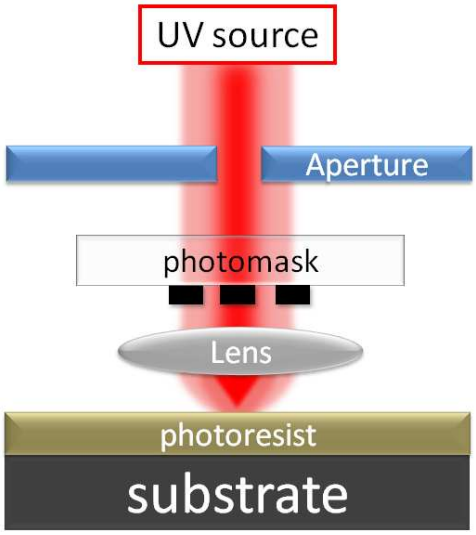
In this study, numerous processing technologies have been used to create metallic nanostructures. Photolithography was used for the pattern transfer of contact pad structures with dimensions in the range of 3μm to 250μm. Electron beam lithography has been used mainly for delivering nanoscale features in the ranging from 12.5nm to 500nm onto various types of substrates.

In the development of semi-metallic nanowire structures, the deposition and milling capability of a focused ion beam has also been investigated. A focused ion beam based Bi nanowire fabrication process has been designed and carried out in the Center for Micro/Nano Science and Technology (CMNST) at the National Cheng Kung University (NCKU), Taiwan.

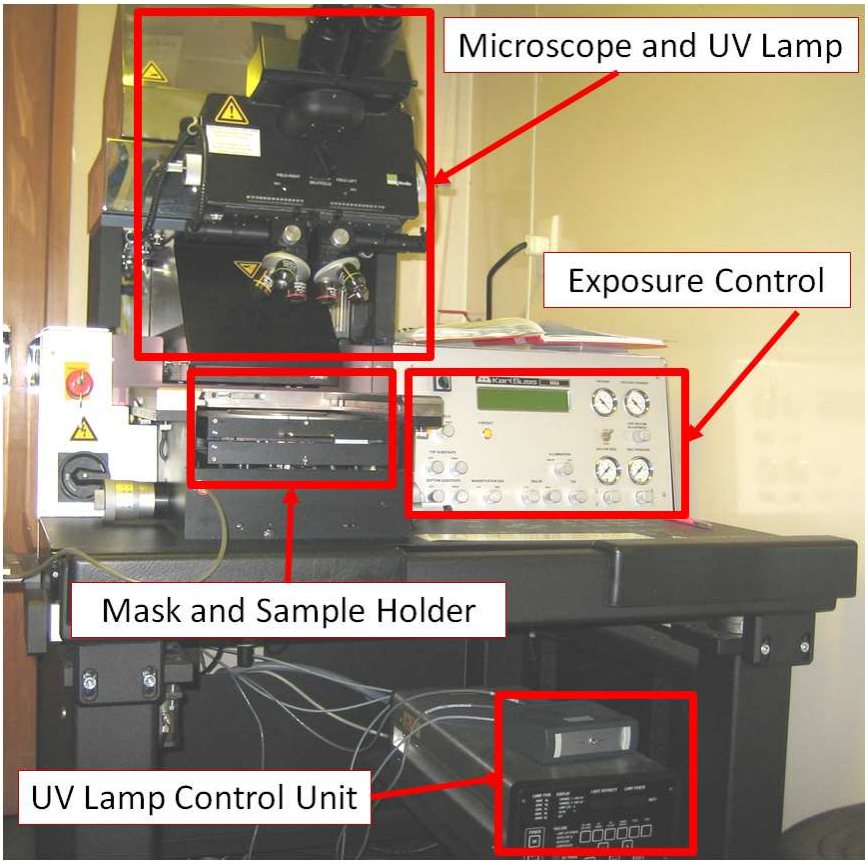
3.2.1 Photolithography and metallisation

The advances in photolithography have been the main driving force of IC scaling as it is the key process in microelectronic fabrication. Photolithography is a pattern transfer technique used to define patterns from a photomask onto photosensitive media using a UV light source. Figure 3.5(a) illustrates a standard photolithography process, where the gap between the photomask and substrate defines the type of optical lithography process. If the photomask is brought in contact with the substrate, it is called contact printing, whereas if the mask is brought near the substrate separated by a small gap, it is called proximity printing.

The photoresist is normally coated onto the substrate using a spinner, where the acceleration, spinning and de-acceleration times that determine resist thickness and uniformity are set according to the type of photoresist used. A single wafer spinner from Laurell Tech Corp. was employed to spincoat photoresist, electron sensitive resist, and conductive polymer material onto 10mm$\times$10mm substrates and four inch wafers.



(a) Key components of a photolithography exposure system.



(b) Suss MA-6 Mask aligner.

Figure 3.5: Photolithography process and apparatus employed for the fabrication.

A mask aligner is an optical lithography system dedicated to mount, align and transfer photomask features onto substrates using UV light. Figure 3.5(b) shows the Suss MA6 mask aligner located at University of Canterbury. This mask aligner is equipped with a 350W Mercury UV lamp source with an intensity of 6.7 mW/cm^2. Prior to any exposure process, the MA6 performs an automated wedge error correction (WEC) mechanism which aligns the two planes of mask and substrates, allowing a homogenous exposure of pattern along the surface of substrates. The Suss MA6 system can be configured to carry out exposure using various contact modes, including proximity, soft, low vacuum, and vacuum contacting modes. This system has been mainly used in vacuum contacting mode to pattern transfer contact pads structures onto photoresist coated substrate prior to the subsequent metallisation process.

3.2.2 Electron beam lithography (EBL)

In the long battle of beating the diffraction limit for lithography technologies, electron beam lithography (EBL) has been the primary successor, capable of creating sub 10nm features on resists. An electron beam lithography system is a maskless direct-write lithography tool that utilises a focused beam of high energy electrons to define patterns on electron sensitive resists. Although electron beam lithography has much higher resolution than conventional optical systems, when it comes to throughput, EBL performs poorly, writing one pixel at a time on the resist. As a result, EBL systems are often used for mask making in IC industry for high precision and high resolution patterning.

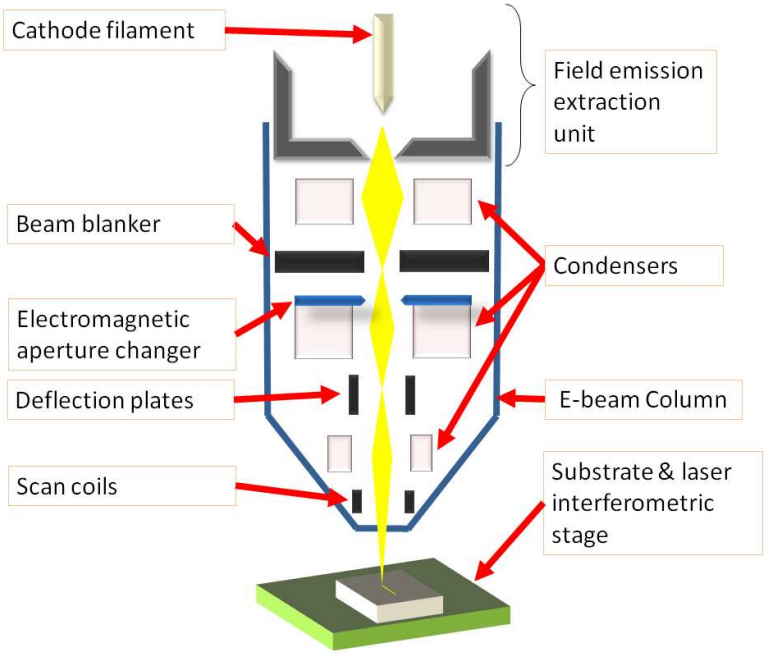
Figure 3.6(a) shows the schematic of internal components in a common field emission EBL system. The source of electron beam systems can come from two types of electron emissions including the thermal emission and the field emission. In a thermal emission system, electrons are extracted from the cathode by heating the filament. Whereas for a field emission system, electrons and are extracted by means of applying a large electric field to the cathode filament. Once an electron beam is generated, it passes through a set of electrostatic, electromagnetic condenser lens, and beam deflection units that focus and shape the beam to a fine spot at the substrate. In a EBL system, although electrostatic

lenses are known to have worse aberration than magnetic ones, they are commonly found at the field emission region as condenser lens, combined with the extractor unit for field emission purpose.

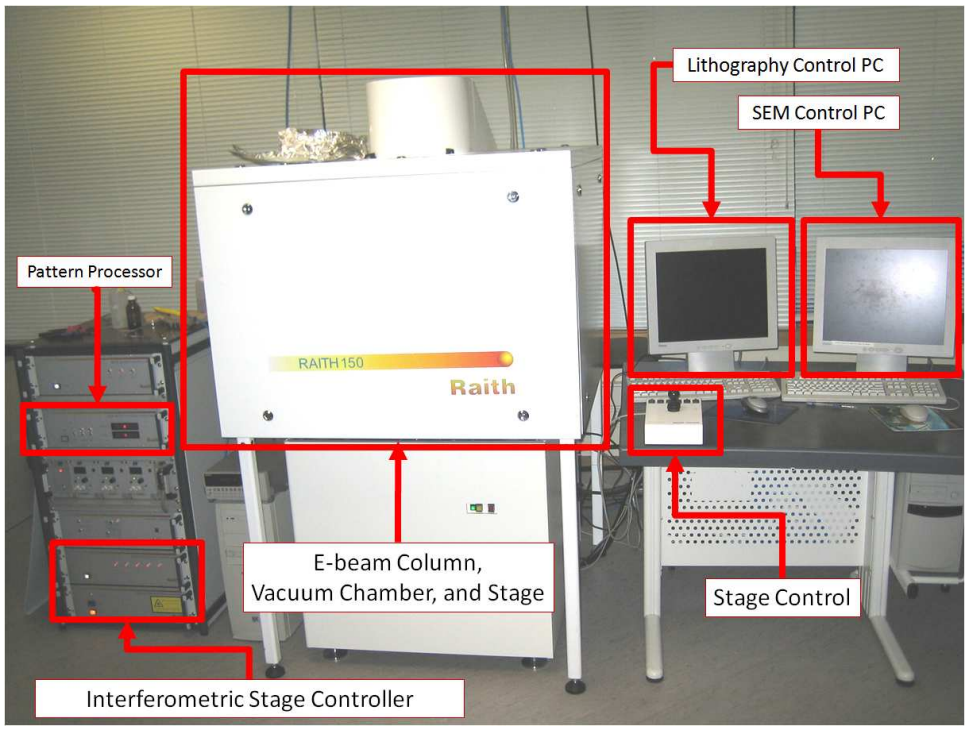
It is necessary to maintain the chamber of an E-beam system at high vacuum to increase the mean free path of electrons, avoiding undesired beam bending and contamination during the exposure process. The beam blanker, scanning coils and deflection units found at the top and the base of the column are normally electronically controlled by high speed hardware and pattern generator for achieving minimum settling and precise exposure times.

Theoretically speaking, the ultimate resolution of EBL is determined by the spherical and chromatic aberrations of the electronic optical system, where a beam spot size in the range of 0.1nm can be obtained [72]. The practical resolution limits of an EBL system, on the other hand, are mainly determined by the combination of exposure, secondary electron backscattering and the subsequent development process [73]. The de-localisation of the exposure process is caused by the coulomb interaction between electrons and resist molecules.

Figure 3.6(b) shows the Raith-150 electron beam lithography system located at the University of Canterbury. It is a fully integrated E-beam system that consists of a LEO 1500 series scanning electron microscope (SEM), laser interferometer stage, high speed pattern generator system and a high vacuum chamber system. In addition, the Raith 150 system is equipped with a robotic sub-chamber loading system that maintains the vacuum level of main chamber, preventing from contaminations during sample loading process. The specifications of Raith-150 EBL system are summarised in Table 3.3[74][75]. Raith 150 has been used extensively to pattern nanoscale structures on polymethylmethacrylate (PMMA) coated substrates including nanowire, and nanotransistor features. The EBL writing strategy, resolution test, exposure details and development parameters will be discussed in the next chapter.



(a) A basic schematic of field emission EBL systems.



(b) Raith-150 EBL facility at University of Canterbury.

Figure 3.6: Electron beam lithography: internal components and apparatus used for fabricating metallic nanowires.

Table 3.3: Raith 150 EBL system specifications.

Filament type	Schottky Thermal field emission
Acceleration voltage	200eV to 30KeV
Probe current	4pA to 10nA
Write field size	1μm to 800μm
Step size	Write-field/65536
Writing speed	10MHz area mode, 2ns resolution
Working distance	2 to 12 mm
Beam diameter	2nm@20KeV, 4nm@1KeV
Sample size	6" automated load lock
Stage	Laser interferometer 2nm resolution
Current stability	0.5% per hour

3.2.3 Reactive ion etching (RIE)

Reactive ion etching (RIE) is commonly used in the IC industry as a high selectivity, anisotropic etching technology. Unlike the isotropic wet-etching process, RIE is a directional etching process due to the presence of ionic species in plasma and biased electric field. In an RIE system, the etching process is initiated by a radio frequency (RF) electric field source operating at 13.56MHz, in which a plasma is generated by the oscillating electric field that ionises the gas molecules into ionised atoms and electrons.

In the vacuum chamber, these electrons are then energised and accelerated toward the opposite direction of the alternating electric field, hitting the walls of the chamber or the electrically insulated wafer platter. When electrons are absorbed into the wafer platter, the electrical charge builds up, resulting in a large negative voltage on the platter at a few hundred volts. The resultant plasma is slightly positive because of the higher concentration of positive ions than free electrons. Due to the voltage difference between negatively charged wafer and positively charged ions in the plasma, ions will drift toward the wafer platter and bombard the surface atoms of the substrate.

The reactive etching process begins when these ions react chemically with the surface atoms and at the same time, physically sputter away the atoms due

to the high kinetic energy of incoming ions. In a parallel plate RIE system, due to the vertical path of reactive ions, anisotropic (vertical sidewall) etching profiles can be obtained with optimised process parameters. In this study, an Oxford Plasmalab 80 Plus reactive etching system at the University of Canterbury has been mainly used to dry etch EBL patterned nanostructures into quartz substrates for the fabrication of imprint molds, where the RIE parameters can be found in Table 3.4.

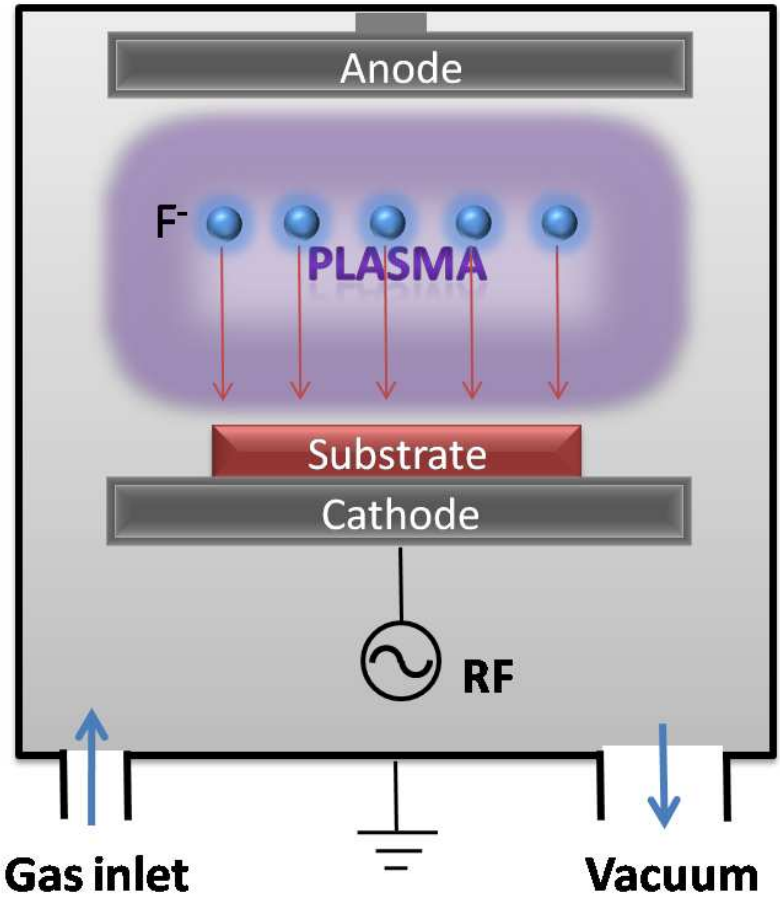
Table 3.4: List of RIE parameters for Quartz etching for nanoimprint fabrication in this study.

Materials	gas	flow rates	RF power	Temperature	etch rate
Quartz	CHF_3/Ar	18%/12.5%	125W	295K	12.5nm/min

3.2.4 Focused ion beam system (FIB)

This part of work related to the use of Focused ion beam systems were performed at the CMNST lab in NCKU, Taiwan. Focused ion beam (FIB) is a innovative maskless lithography system that utilises a focused beam of Ga^+ ions for sputtering and depositing of materials on the substrate surface. FIB systems have been widely used in various fabrication and analysis process including direct-write lithography, transmission electron microscopy sample preparation (TEM), IC failure analysis, microelectronic circuit modification, micromachining, and direct material sputtering or deposition.

FIB system operates similarly to a scanning electron microscope system, where a liquid metal ion source (LMIS) has been employed to provide sources of ions a few nanometres in radius. Gallium is the most common source for LMIS due to its low melting points (29.8°C), low volatility at the melting point, low vapor pressure that allows Ga to be used in its original form, and its emission characteristics that give high angular intensity with a minimum energy spread. Inside the ion column of FIB system, Ga+ ions can be accelerated with an acceleration voltage ranging from 5 to 30KeV and a typical beam current of 1pA to 20nA can be set in the FEI nanolab nova-200 system (As shown in Figure 3.9(a)).



(a) Schematic of a parallel plate reactive ion etching systems.

(b) Oxford Plasmalab 80 Plus reactive ion etching system.

Figure 3.7: Reactive etching process and system.

The milling process in a FIB takes place when an energetic ion beam sputters away the materials of the target, transferring the momentum from the incident ions to the target atoms. A surface atom is ejected into the vacuum chamber as a sputtered particle when the received kinetic energy overwhelms its surface bonding energy of the target material. During the milling process, the surface of substrates might suffer from a certain degree of amorphisation damage due to the irradiation of the ions. As a result, it is important to choose a substrate that would receive the least damage from the bombardment of excess Ga ions.

FIB allows material deposition on almost any surface with relatively high spatial precision. There are generally two ways of material deposition in FIB, the ion beam induced deposition and the electron beam induced deposition. For any of these depositions to occur, precursors that are heated and injected to the surface of the target must have enough sticking probability to the desired area in sufficient quantity. Moreover, it must decompose more rapidly into the desired material than it is sputtered away by the ion beam [76]. The electron beam deposition in dual beam systems are commonly used for depositing conductive and insulating layers.

Dual beam FIB systems that incorporate both a scanning electron microscope (SEM) column and a focused ion beam (FIB) column have become more and more popular over the last decade due to their ability in imaging the substrate with an electron beam without the concern of sputtering away surface materials by ion beam. Figure 3.8 shows an image containing key components in the vacuum chamber of FEI nanolab nova-200 FIB system. In most dual beam platforms, the electron beam columns are located normal to the substrate surface and the ion beam column are at 52° to the surface plane. In dual-beam FIB, all of the electron beam column, ion beam column, and gas injection system share the same coincident point, allowing the focused beams and precursor gas flows to intersect with each other at the same point on the sample [76].

Two FIB systems have been employed, including FEI nanolab nova-200 and SMI-3050. Both of these FIB machines are dual-beam system that incorporates 30KeV Ga^+ ion beam and field emission electron beam for milling and deposition purposes. The FEI nanolab nova-200 and SMI-3050 FIB systems are located

at the National Cheng Kung University (NCKU) and the National Sun Yat-sen University (NSYSU) in Taiwan. The SMI-3050 (as shown in Figure3.9(b))system has demonstrated the world's smallest ion beam diameter of 4nm and it is equipped with a 5-axis motorised eucentric tilting stage and a auxiliary chamber.

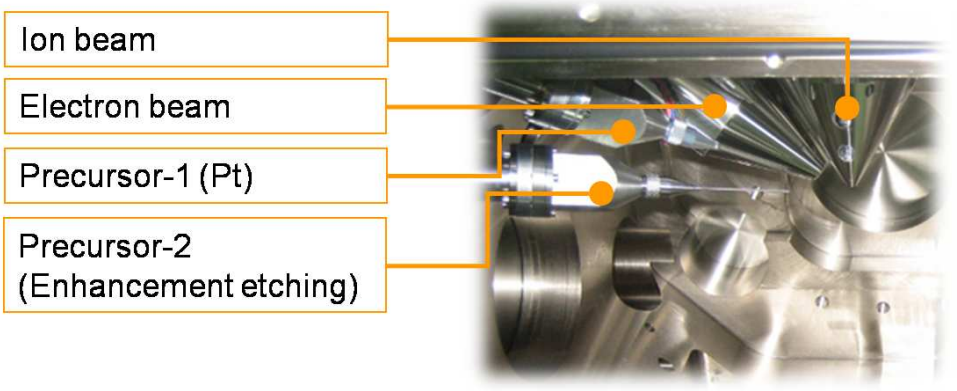
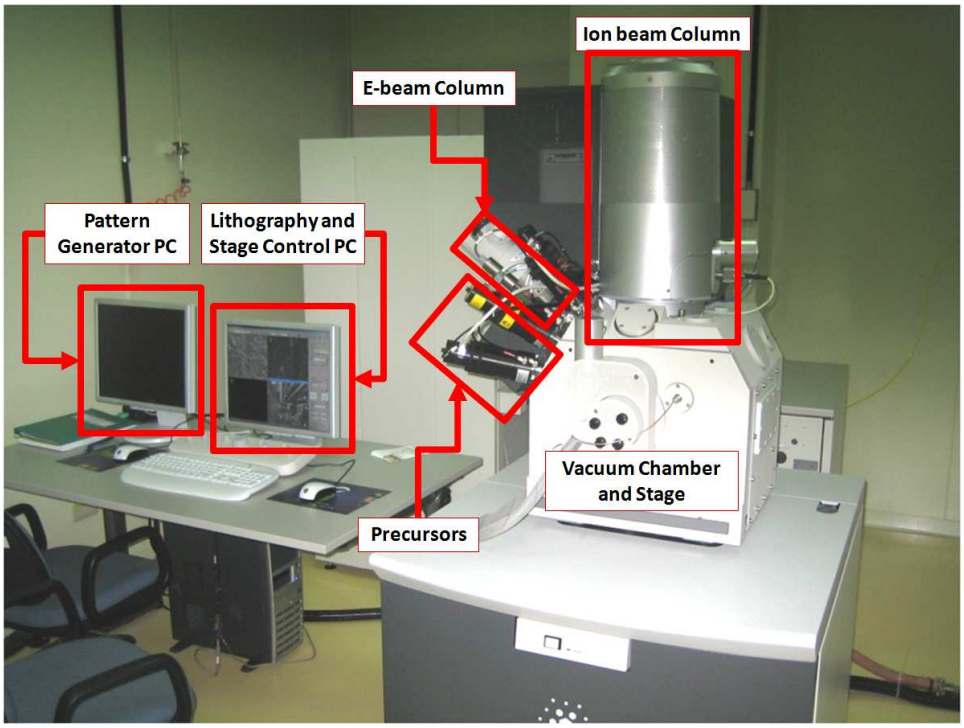


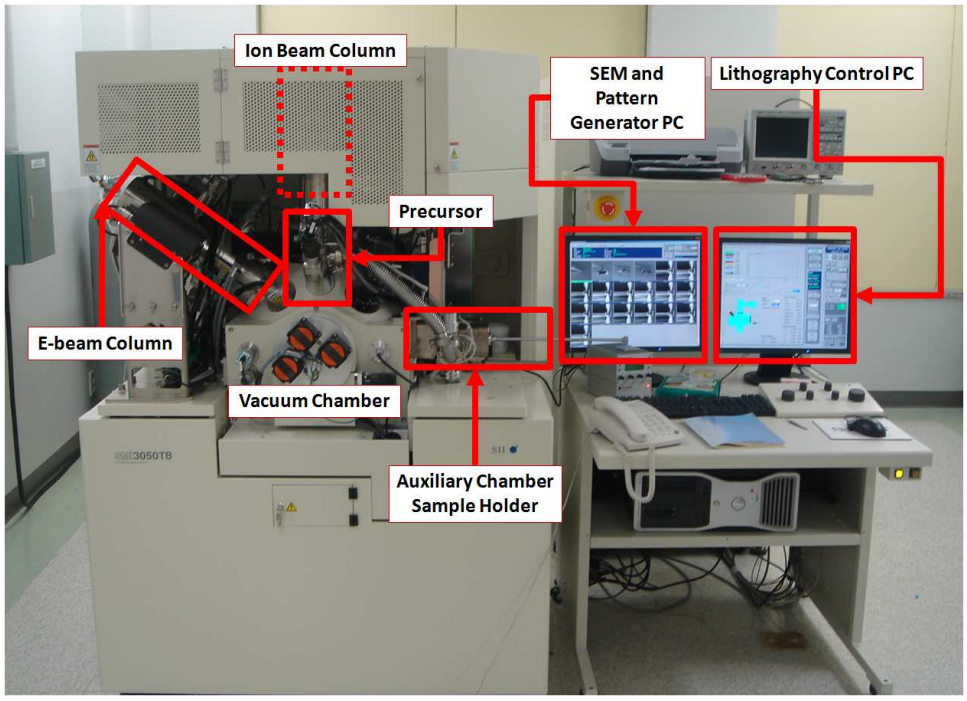
Figure 3.8: Vacuum chamber and key components in a FEI nanolab nova-200 FIB system.

The FEI nanolab nova-200 is a newer generation FIB system, which offers a more user-friendly interface and a high resolution field emission SEM column with monopole magnetic immersion final lens. The achievable ion beam and electron beam diameters for this FEI system are $1nm$ and $5nm$. Although this FEI system is not equipped with an auxiliary chamber, it is equipped with a broader range of precursor gaseous including platinum, carbon, enhanced insulator etching, and enhanced semiconductor etching. Whereas for SMI-3050 system the only two precursors installed are for the deposition of tungsten and SiO_2. In addition, FEI-200 FIB systems supports greyscale bitmap format data for 3-D milling, where the dosage can be controlled easily by the greyscale factor.

In this study, FIB systems were mainly utilised to mill bismuth thin films into nanowire structures, followed by in-situ depositions of platinum or tungsten contact electrodes. To investigate the deposition and milling capabilities of these systems, they have also been employed to mill Pt, W structures and quartz substrates.



(a) FEI nanolab nova-200 focused ion beam system.



(b) Seiko SMI-3050 focused ion beam system.

Figure 3.9: Dual beam Focused ion beam systems employed for the fabrications.

3.3 Characterisation technologies

In this study, a variety of techniques have been employed to characterise the physical and electrical properties of nanoscale devices. When it comes to nanoscale structures with dimensions smaller than 200nm, optical microscopes can no longer be used to resolve images of these features due to the diffraction limit of light [77]. There are a number of ways of imaging these nanostructures beyond the wavelength of light including scanning electron microscopy, scanning probe microscopy, and transmission electron microscopy. Among these techniques, atomic force microscopy (AFM) has been used on the surface morphology of deposited films and nanoscale structures. Scanning electron microscopy (SEM) has been used extensively to determine the dimensions of various micro and nanoscale structures and to align the EBL pattern to the contact pads prior to exposure.

In terms of electrical characterisations, semiconductor parameter analysers have been employed to evaluate the I-V results and external source devices have been used to supply the gate voltages to the lateral metal gates in the nanotransistor device.

3.3.1 Scanning electron microscopy (SEM)

Most EBL systems are built and operated based on scanning electron microscopes, which provide the sources of focused electron beams with either thermal emission or field emission guns controlled by a series of electrostatic or electromagnetic lens. Imaging in a SEM system is created by the detection of secondary electrons by raster scanning the sample surface with a fine electron beam at high acceleration voltage. In the SEM system, when the incident electron beam strikes the sample, secondary electrons are generated within few nanometers from the sample surface due to their low energy[78]. The collection of secondary electrons emission data contain two-dimensional intensity distribution of the scanned field and can be used to represent the surface topology of the sample. In addition, recent SEM systems are often equipped with energy-dispersive X-ray (EDX) attachments that detect x-ray emission of the interaction

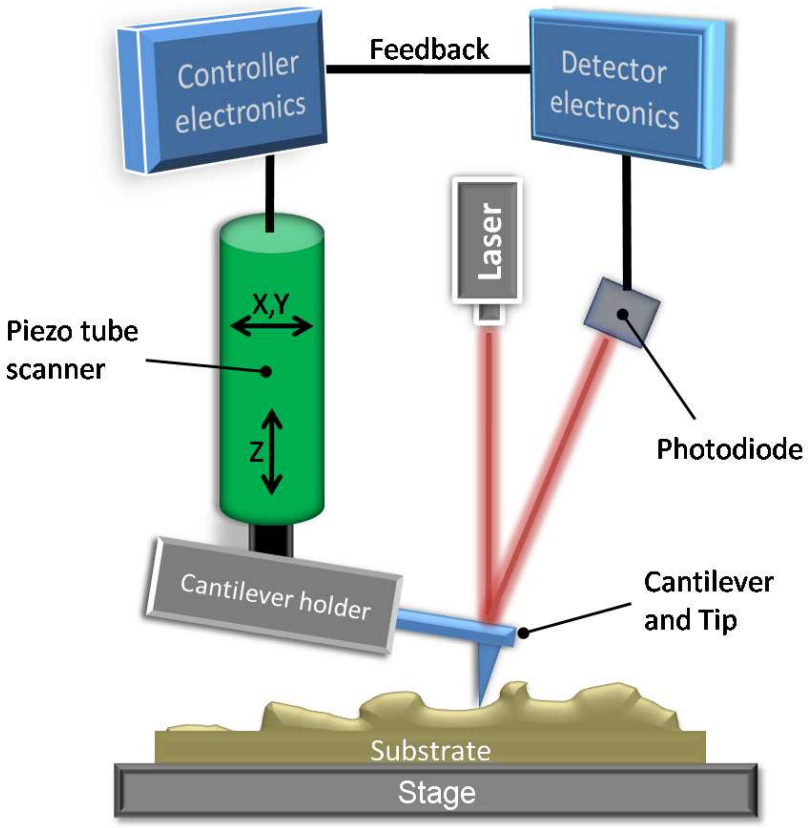
of electron with the sample surface. The EDX is a type of spectroscopy that can be used to analyse the chemical composition for the sample surface.

In this work, Raith 150 EBL system, FEI nanolab nova-200 and SMI-3050 FIB systems were used extensively as lithography and SEM tools to examine and characterise the physical structures of fabricated features. The dualbeam FIB systems allow real time SEM imaging during the milling process and the SEM column of Raith 150 is an essential feature when it comes to the alignment of contact pads and nanostructures prior to the E-beam exposure process.

3.3.2 Atomic force microscopy (AFM)

An atomic force microscope is one type of high resolution scanning probe microscope capable of delivering images with resolution of fractions of a nanometer scale. Since its invention in 1986, AFM based imaging system remains among the highest resolution with sub-nanometer 3D imaging capabilities nowadays[79]. It is a mechanical probe scanning and imaging system operate by measuring the forces between the sharp tip of a cantilever and the surface material of the substrate. In an AFM system, depending on the types of operation and attachments provided, a variety of forces can be measured including contact force, magnetic forces, Van-der-Waals forces, capillary forces, chemical bonding and electrostatic forces etc[80]. These force measurements contain valuable information about the surface material and some of the forces can be used to plot the high resolution surface topology in a 2D or 3D manner. Figure 3.10(a) represents the operation and key elements in an AFM system, where the forces are measured through the tip attached to a cantilever that can be positioned at close proximity to a contact on the surface material. During the measurement process, the deflection or oscillation caused by the interacting force is measured by the reflected laser signal from the top of the cantilever into a photodiode unit. This signal is then analysed in the computer and then fed back to the controller that manipulates the movement of the piezo-electric tube, which moves at vertical (Z-axis) direction to maintain a constant force between tip and surface, and moves horizontally (XY-axis) to scan the entire the substrate.

Figure 3.10(b) shows the head unit of a Digital Instrument 3100 AFM sys-



(a) Components in an a atomic microscope.

(b) Head unit of Digital instrument 3100 AFM system.

Figure 3.10: Atomic force microscope: key components and the system used in this study.

tem, which was employed to image and measure the size and surface topology of fabricated nanoscale features and deposited films. This system allows three modes of operation, which are: contact, non-contact and tapping modes. In contact mode operation, the tip raster scans the substrate by simply dragging the tip of the cantilever across the surface, introducing a large force to be measured and computed in the system. In order to prevent the tip of the cantilever to collide or snap into the surface of the substrate material, the movement of the cantilever is controlled by a piezo-electric tube in a way that a constant force is maintained between the tip and surface. In the non-contact mode operation, the cantilever is at first oscillating near its mechanical resonance frequency, where the amplitude, phase and resonance frequency components of this oscillation are modulated by the interaction force as the tip oscillates right above the surface of a material[81].

In this study, all the AFM measurements were carried out in tapping mode. This allows a more accurate data collection without having the risk of damaging the tip and sample as compared with contact mode operation[81][82]. Three types of cantilevers were used to assess the topology for this work, these are the NSC-14, STING, and NSC-11. The AFM parameters and physical properties for these tips can be summarised below in Table 3.5.

Table 3.5: Physical properties of AFM tips used in this study.

Type	Tip radius(nm)	Resonance frequency (kHz)	Force (N/M)
NSC-14	10	160	5.0
NSC-11	10	60	3.0
DP14/STING/AlBS	2.4	160	5.7

3.3.3 Electrical characterisation technologies

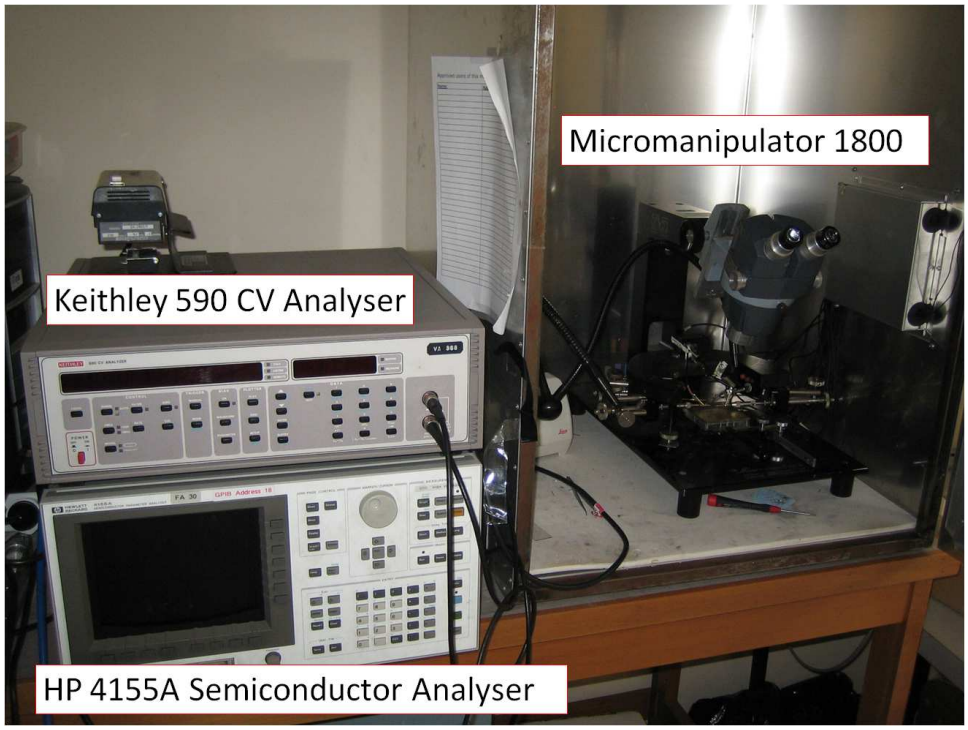
In this work, a number of electrical measurements were carried out to determine the electrical properties for a variety of metallic and semimetallic nanowires. This has allowed us to observe any size dependent effects on electron conduc-

tion in a confined channel. Several electrical characterisation techniques were employed, including the transmission line measurement analysis, two point and four point resistance analysis, and the gate effect or conduction reduction effects for metallic nanowire under the influence of gate voltages.

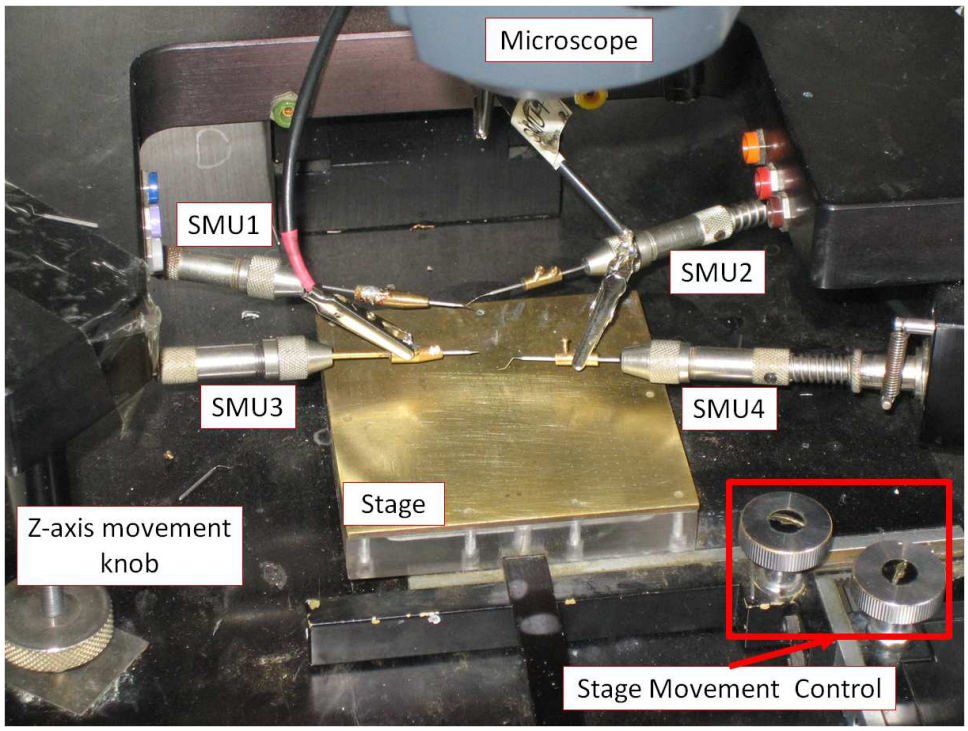
For the electrical characterisations, HP4155A semiconductor analyser, Keithley 2400 source meters, and Keithley 4200 semiconductor analyser have been employed.

HP4155 semiconductor analyser, located in the Electrical Engineering department of the University of Canterbury have been used extensively for conduction measurements including resistance measurement and electric field effect, and leakages of nanowire transistor structures. It has four high accuracy source/monitor units (SMU), two voltage source units (VSU), and two voltage measurement units (VMU). All of the measurements were carried out in an aluminium shielded box, where a probestation, the Micromanipulator 1800, has been employed for connecting the semiconductor analyser probes to the bonding pads as small as $70\mu m^2$ through its four manipulators. In terms of sweep control, HP4155A offers three settings for the integration time for the measurements, which are short (640μs), Medium (20ms), and Long (greater than 320ms). Long integration time and double sweep setting has been used in this work for high sensitivity and low resistance measurements of metallic nanowires. This has the effect of improved signal to noise (S/N) ratio during the data acquirement of high sensitivity measurements. Keithley 4200-SCS[‡], located at the Material Science department, National Cheng-Kung University (NCKU), Taiwan, was employed for the electrical characterisations of bismuth nanowire devices.

[‡]The specifications and images are available from Keithley Instrument Inc website, http: www.keithley.com.



(a) HP4155A semiconductor analyser and Micromanipulator 1800 probe station in Al shielded box.



(b) The closeup view of Micromanipulator 1800 probe station and its setup of four probes.

Figure 3.11: Semiconductor parameter analyser and probe station used in the electrical characterisations of metallic nanowire devices.

3.3.3.1 Transmission line measurement (TLM)

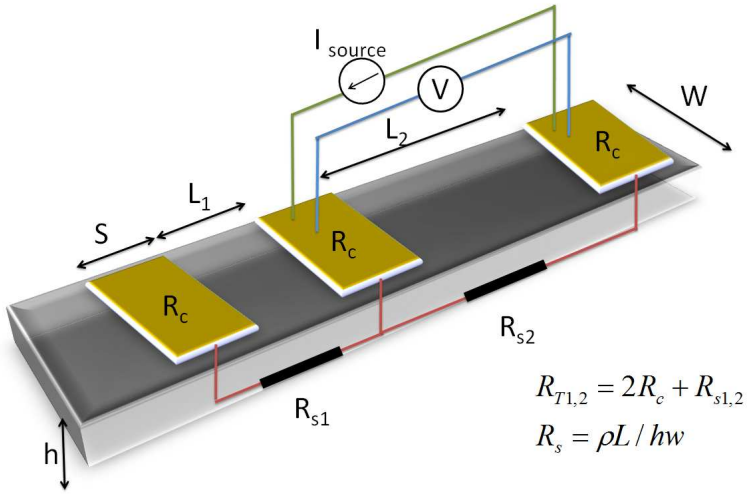
Transmission line measurement (TLM) is an electrical characterisation method originally proposed by Shockley in 1964 [83]. This characterisation technique involves the use of a number of metal contacts separated by known distances on the semiconductor material. By using a current source and voltage meter to measure the resistance for each pair of the contacts, a function between the measured resistances versus the contact separation distance can be plotted. The slope of this plot represents the sheet resistance and the intercept point at the Y-axis represents two times the contact resistance. This technique offers a quantitative method for measuring contact resistances that determine the performance of ohmic contacts to semiconductors.

However, in Shockley's TLM model, the sheet resistances beneath the ohmic contact between metal and semiconductor have not been taken into account. A more accurate model was later developed and published by Reeves and Harrison in 1982[84]. Figure 3.12 shows the simple schematic for layout of a TLM analysis, where the total resistance is contributed by the contact resistance and resistance of semiconductor wire. For simplicity, the sheet resistance beneath the contact in this section was excluded. TLM analysis was carried out to determine the ohmic contact resistance and the sheet resistance for the nanowire structures in this study. The four contact pads were deposited and patterned onto a section of nanowire using electron beam lithography and thermal evaporation based metallisation processes.

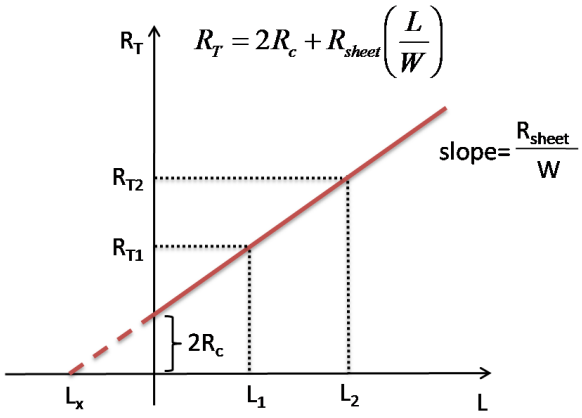
3.3.3.2 Two point and four point resistance measurement

In a two point resistance measurement, either a current source or voltage source can be used to determine the corresponding voltage drop and current flow through a section of nanowire separated by contact electrodes. This allows the calculation of total resistance including the contact resistance and nanowire resistance. In order to accurately measure the resistance for a nanowire, a four-point resistance measurement can be performed. It is normally carried out in a way that the middle two contacts are probed through a voltage meter, whereas the outer two contact electrodes are connected with a constant current source.

By dividing the voltage drop across the middle two contacts with the supplied current, the nanowire resistance can be obtained accurately without the influence of contact resistances.



(a) Schematic diagram of the transmission line measurement setup for contact and sheet resistance of materials, modified from Reeves and Harrison[84].



(b) An example of TLM plot and the functions.

Figure 3.12: Transmission line analysis, setup schematic and a typical resistance versus length plot.

Chapter 4

Fabrication of metallic nano structures

The main goal of this project is to fabricate and synthesise the smallest metallic nanowires using controllable and repeatable approaches to allow us to study and examine the electrical properties and to explore the gate effects of these structures.

First studied was the fabrication of metallic nanowire structures using EBL. The optimised exposure parameters were determined experimentally to allow for the fabrication of sub 20nm wide metal nanowires. Next, the fabrications of ultra thin metal film structures were explored. RF sputtering was employed for the deposition of high quality and thin Ag film with thicknesses ranging from 7nm to 20nm.

In order to perform gate effect measurements on these devices, lateral gate structures were fabricated in close proximity to the ultra thin nanowire structure separated by air gaps as narrow as 20nm. Having gate electrodes so close to the nanowire structures has imposed great fabrication challenges in EBL. To address these issues, both of the gate and nanowire structures were defined on PMMA using single pixel line exposure technique. The widths of air gaps can be controlled by both the dose and the designed layout.

The nanowires were made as narrow as possible to allow detections of any changes in conduction and the possibility of electron depletion by the applied fields. For the development of the narrowest possible wires, numerous chal-

lenging issues were encountered, including the severe charging effect of EBL writing on insulating substrates, proximity effects that affect the physical dimensions of nanowire and gate structures and the development and the metallisation processes that yield continuous and conductive wires for electrical measurements. Considerable effort has been made to yield the EBL process for defining and fabricating metallic nanowire at a high resolution and controllable manner. Nanowire structures a few microns long, with widths ranging from 200nm down to 12.5nm have been successfully fabricated using Ag, Al, and NiCr.

Due to the difficulties involved in reducing the linewidth under the 12nm node, the fabrication of sub 10nm Ag thin film structures has been developed using photolithography and RF sputtering techniques. Unlike nanowires, the only dimension considered to be in the nanoscale range for a Ag thin film structure is its thickness. In the experiment, RF sputtering has allowed us to coat a continuous and conductive film as thin as 7nm on Si_3N_4 substrate. The top gate and dielectric for this structure were deposited using electron beam evaporation and RF sputtering.

This chapter details the pattern design, fabrication processes, and experiments involved in the development of metallic nanowire and thin film structures on insulating substrates. First covered is the fabrication of contact pads used for connecting external testing probes to the nanowire structures. This is followed by the fabrication of metal nanowires with gate structures. Finally, the fabrication of Ag thin film device with top gate structure is described. The characterisations of these nanowires and thin film structures will be presented in detail in Chapter 6.

4.1 Substrate preparation

In order to characterise the nanowire based devices electrically, insulating substrates must be used. SiO_2 and Si_3N_4 coated Si wafers were common insulating materials used as the base substrates for device fabrication and characterisation. The specifications of these wafers are given in table 4.1.

Table 4.1: List of substrates used in this study.

material	Size	thickness	base substrate	orientation	Ω/cm
SiO_2 thermal	4" wafer	$1\mu m$	Si P-type	100	7-13
Si_3N_4 LPCVD	4" wafer	$1\mu m$	Si N-type	100	3-6

Due to the large number of samples required for EBL and FIB experiments, samples were first cleaned and processed as four inch wafers. They were then cut into 10mm by 10mm squares after the fabrication of contact pads were completed. The surface preparations of samples play an important role in the film and resist coating processes. Extra care must be taken to reduce the substrate contamination, as this would lead to undesired short circuit and adhesion problems. A standard cleaning protocol has been followed on all of the samples prior to and after the processes. This includes first the immersion and sonicating with Acetone, Methanol, Isopropyl Alcohol (IPA), followed by drying with N_2 gas, baking at 95°C in oven, and visual inspection under the optical microscope. In addition, glow discharge was carried out using the Blazer 510A thermal evaporator plasma source at a low pressure environment to treat and clean the surface of the four inch wafers prior to the fabrication process. It was used as a final step of bare wafer cleaning to improve the surface condition and adhesion for the metallisation process [85]. Other substrates such as Quartz or Si have been used for nanoimprint mold fabrication, focused ion beam milling and bismuth thin film deposition experiments.

4.1.1 Gold contact pads fabrication

Gold electrodes and bonding pads were used as interconnects for nano devices fabricated on insulating substrates, allowing easier alignment of patterns in

PMMA during the EBL process due to the pronounced emission rate of secondary electrons. In this study, photomasks containing contact pads features were designed using Tanner L-edit v12.6, a PC-based layout editor from Tanner Research [86]. The patterns were transferred onto substrates using optical photolithography and subsequent metallisation processes.

In the design, micro-contact structures were formed by a multiple number of 5μm wide wires designed to allow different functionality and characterisation techniques for device operation. The bonding regions of these contact structures were made 200 μm by 200 μm in size, designed to accommodate external wire bondings to PCB and direct probing using the HP-4155A probe station.

4.1.1.1 Photolithography process

Figure 4.1 shows the fabrication steps of the photolithography process used for the definition of contact pads. Both the positive and negative photoresists have been used to pattern the dark-field and light-field photomasks containing the required patterns. Table 4.2 shows two types of photoresists used in this study, the positive AZ1518 (manufactured by Microchemicals .GmBH) and AZnLOF2020 (manufactured by Microchemicals, thinned from AZnOF2070 by AZ1500 thinner). This negative resist exhibits high contrast property during development, suitable for high aspect ratio patterning and lift-off purposes[87][88].

In the contact pad fabrication process, right after the photoresist was spun onto the 4 inch wafer, it was softbaked on a hotplate for 2 min at 110°C prior to UV exposure. The exposure was carried out using the Suss MA6 mask aligner at 350W UV for a duration of 30s to 60s depending on the resists used. The exposed samples were developed in AZ MF300 developer and rinsed with deionised (DI) water. Prior to the metallisation process, the wafer was cleaned in a 500W oxygen plasma asher for 30s to remove organic materials on the substrate and to improve the adhesion to substrate for the evaporation process.

The metallisation of gold contact pad structures consists of thermal evaporation of 10nm of NiCr as an adhesion promoter and 40nm of Au, followed by the subsequent lift-off process. A bi-evaporation process in the Blazer 510 thermal

Table 4.2: List of photoresists and their exposure parameters.

Resist name	AZ1518	AZnLOF2020
Resist type	positive	negative
Thickness	1.8μm	2.0μm
Coating parameters	1min@4000rpm	10s@500rpm then 30s@4000rpm
Softbake	2min@110°C	2min@110°C
Exposure (350W)	60s	30s
Post-exposure bake	not required	1min@120°C
Development (MF300)	30s	1min

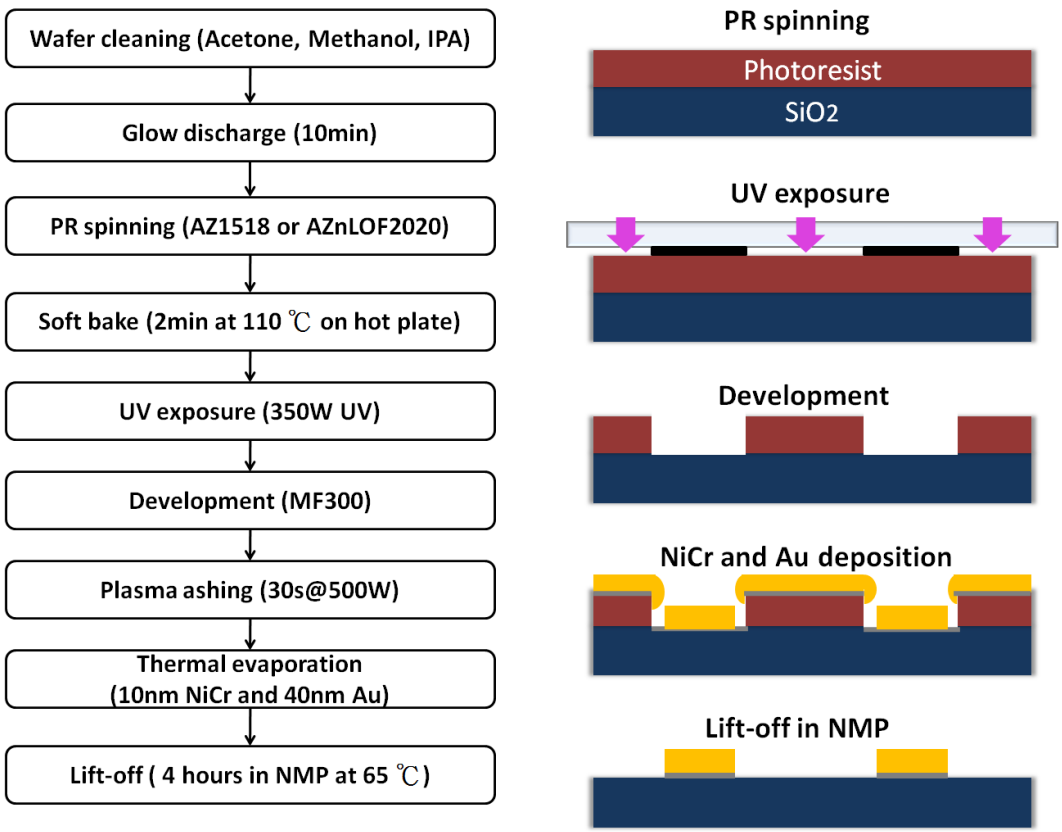
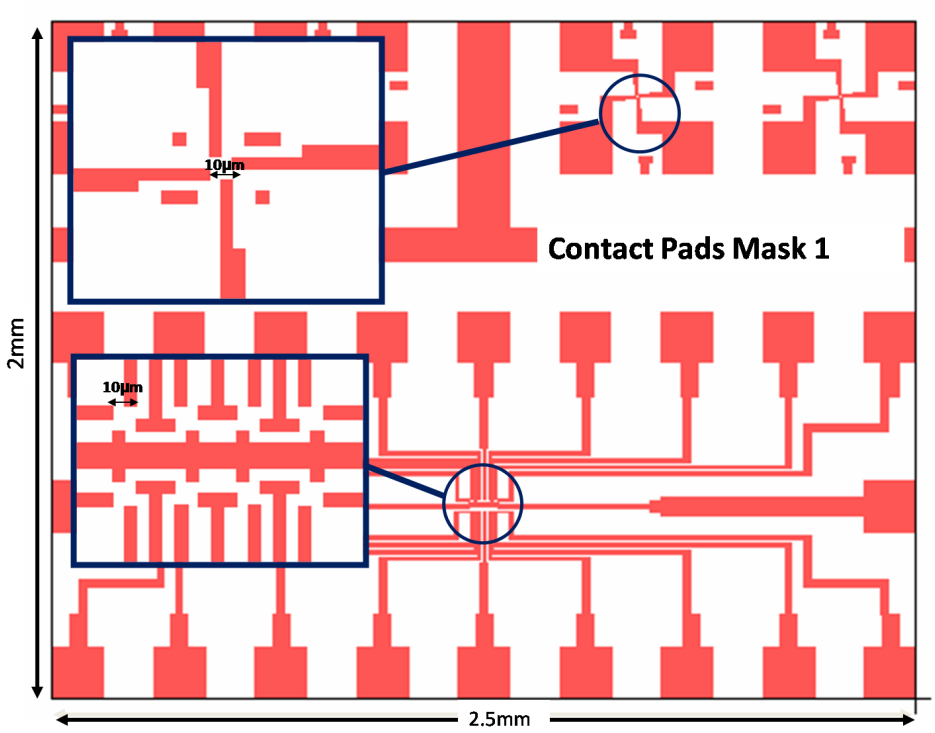
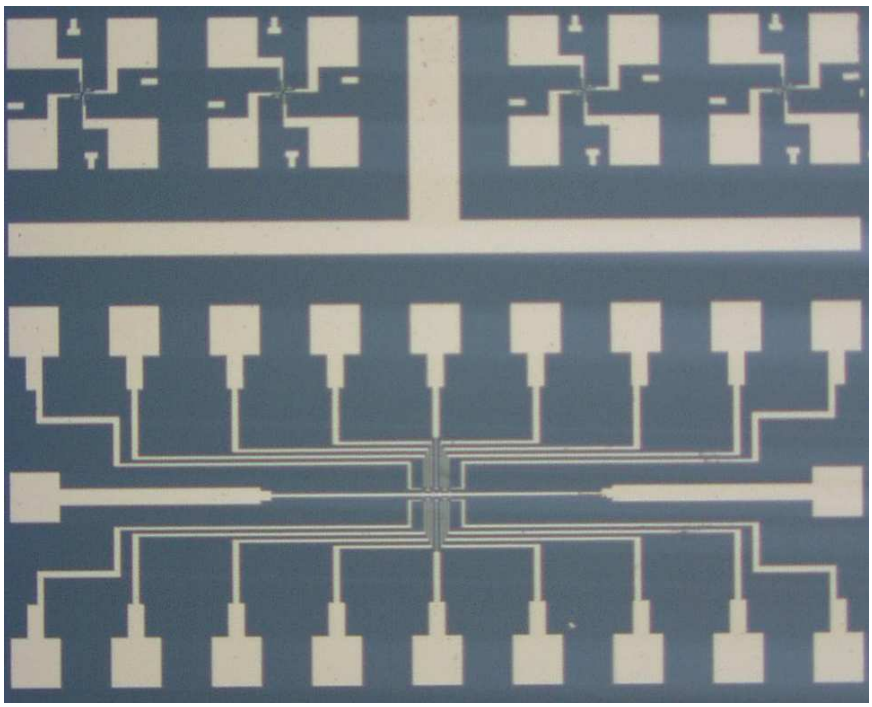


Figure 4.1: Contact-pad fabrication and photolithography process.

evaporator was employed to deposit 10nm of NiCr (99.99%)and 40nm of Au (99.99%) onto the wafer respectively without breaking of the vacuum. After the evaporation process, the lift-off of contact pads were carried out in N-Methyl-2-Pyrrolidone (NMP, manufactured by Microchemicals) remover at 65°C for 4 hours, followed by sonicating for 30s in the ultrasonic bath, rinsing in DI-water for 30s, drying with N_2 and finally, placed in a oven for 30min at 95°C. Figure 4.2 shows one of the photomask design used in this work and its corresponding Au contacts structures. The processed 4 inch wafers were later cut into 10mm by 10mm square prior to the EBL based processes.



(a) Photomask design of contact pads.



(b) Image taken by optical microscope showing the implementation of photomask design on insulating substrate using 50nm of Au and 10nm of NiCr.

Figure 4.2: Photomask design and the fabrication result of gold contact pads.

4.2 Electron beam lithography process of nanowire structures

Previous section covers the fabrication steps for contact electrodes and bonding pad on substrates. Metallic nanostructures were aligned and patterned in a way that makes good electrical contacts to these contact electrodes during the EBL process. In order to deliver the smallest possible metal nanowire features on PMMA on insulating substrates, experiments used to determine the E-beam exposure and resist parameters were performed for each type of nanowire structures. The fabrication process for metallic nanostructures can be summarised as Figure 4.3. First, a 10mm by 10mm substrate with pre-defined Au contact electrodes was cleaned by immersion in acetone and IPA in ultrasonic bath for 30s followed by drying with N_2 gas and heated on a hot plate at 95°C for 2 min. The sample was then cleaned in plasma asher at 500W for 2 min to remove any organic materials prior to the PMMA* spincoating process. The PMMA coated sample was then soft baked at 185 °C for 30 min in oven, followed by EBL patterning in Raith-150. The development of EBL exposed PMMA samples were carried out in MIBK:IPA 3:1 solution at 23°C for 31 seconds. In this work, we have employed ultrasonic assisted development process for sub 13nm wide nanowire patterns on PMMA. Thin layer of metal film was deposited on the developed sample using either thermal evaporation or electron beam evaporation, and the lift-off process was carried out in NMP at 65°C for 4 hours.

4.2.1 EBL pattern design

Raith 150 was employed for defining nanowire and micro-contact structures that overlay on top of the pre-defined Au contacts. Nanostructure patterns dedicated for four-point resistance, TLM, and gate effect measurements based on nanowires and Y-branch structures were all created in GDS-II (Graphic data system) format using Tanner EDA L-edit v12.6.

These GDS-II patterns contain information about structure dimensions and

*The parameters of PMMA used in this study will be covered in Section 4.2.3.

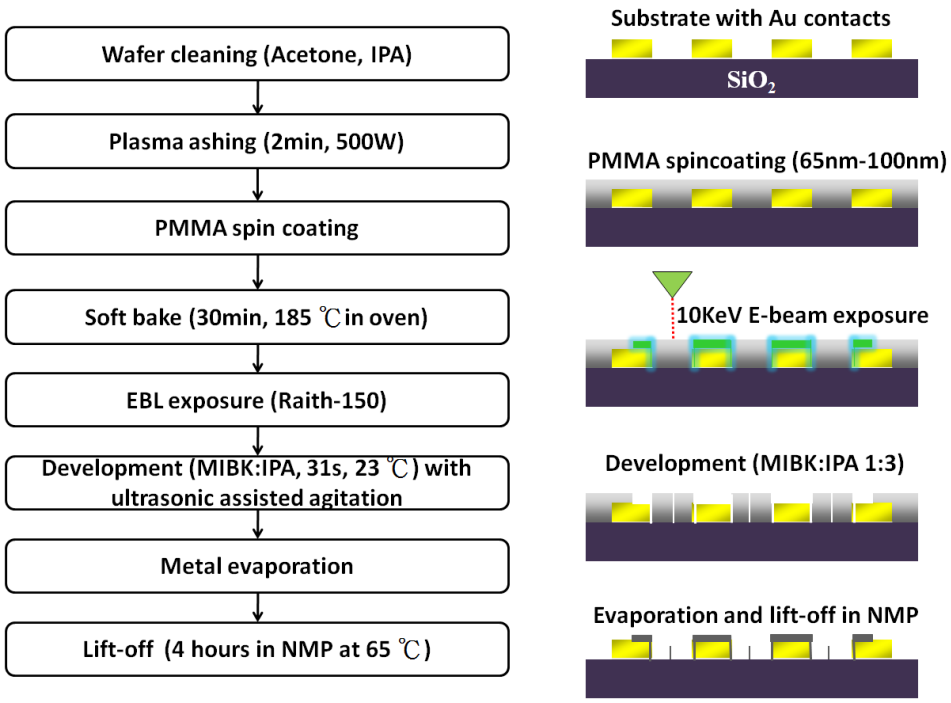


Figure 4.3: Electron beam lithography process for patterning nanoscale features on insulating substrates.

coordinates, GDS-II coded layer numbers, exposure sequences and dose parameters. In the design of EBL patterns, three layers were used including contact pads to micro-contact layer (layer 3), micro-contact to nanowire layer (Layer 2), and the nanowire layer (Layer 1). During the EBL process, these three layers of GDS-II pattern were exposed sequentially from layer-1 to layer-3 respectively. Figure 4.4 shows the GDS-II design for the micro-contact layer responsible for overlaying and connecting the nanowire and gate structures (Figure 4.4 (b))to the photolithographically defined Au contact pads (Fig 4.4(c)). In the design, each micro-contact electrode has exactly the same area size for the consistency of contact resistances during electrical measurements.

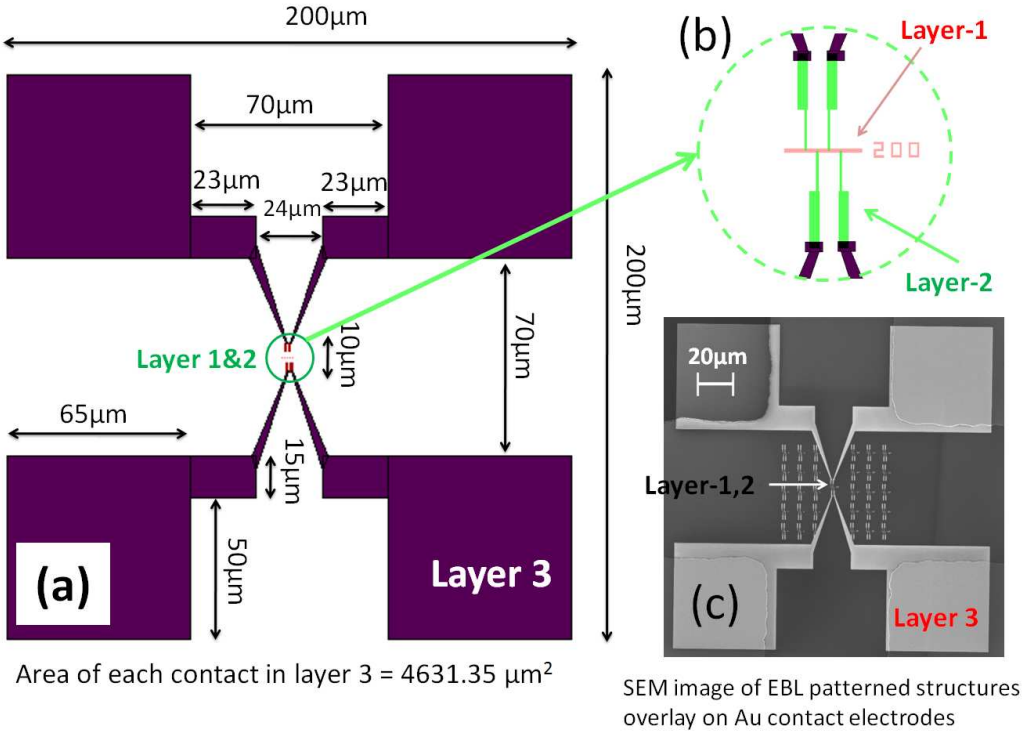


Figure 4.4: Micro-contact and nanowire patterns designed for EBL exposures of nanowire characterisation structures: (a)GDS-II pattern design of micro contacts (Layer 3) that connects external Au contact to nanostructures.
(b)The close up of nanowire structure used for 4 point measurement containing 200nm wide, 4μm long nanowire (Layer 1) and its interconnects to micro-contacts (Layer 2).
(c)SEM image of micro-contacts and nanostructure pattern overlay on Au contact pads formed by EBL exposure at 10KeV and development in MIBK:IPA solution.

Figure 4.5 shows the GDS-II designs for layer-1 and layer-2 made to perform resistance measurement. Figure 4.5(a) shows the four point measurement layout for a 200nm wide nanowire and Figure 4.5(b) shows the design for single pixel line nanowire. Single pixel lines in GDS-II were employed to deliver the smallest possible nanowire features on PMMA. Figure 4.6 shows the GDS-II patterns for layer-1 and layer-2 structures for metallic nanowire based structures for gate effect measurements, including an electrostatic nanowire and gate structure (Fig 4.6(b)), and the Y-branch nanowire device (Fig 4.6(a)). The dimensions of these wires and micro-contact structures were arranged in a way to allow high accuracy alignment ($\pm 0.2\mu$m) to contact pads.

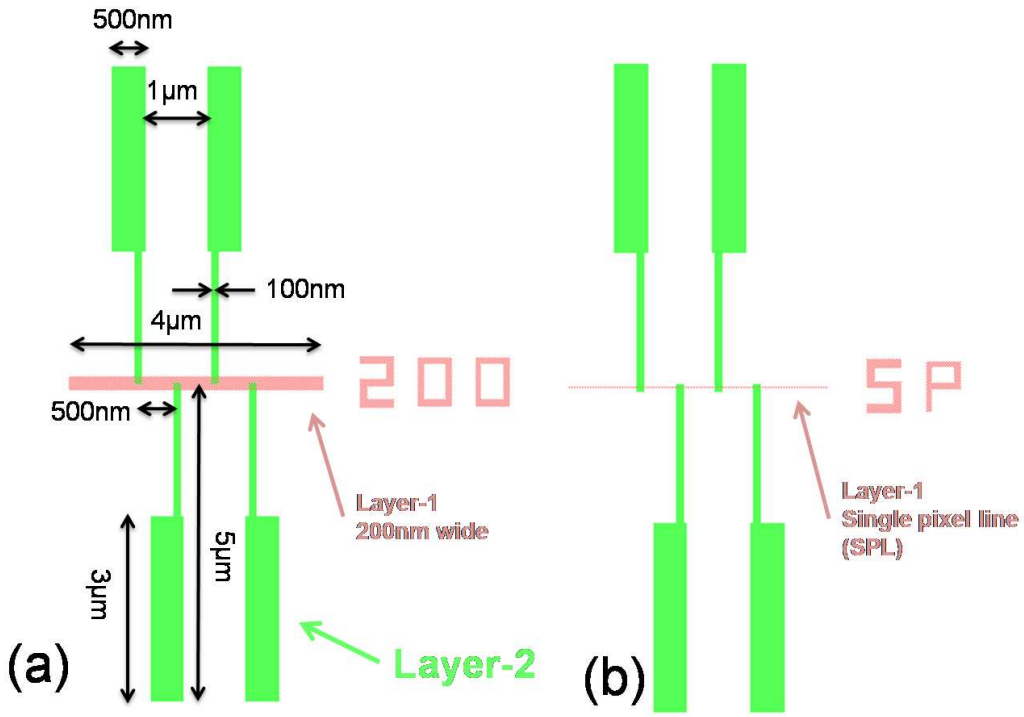


Figure 4.5: GDS-II pattern for four-point and transmission line (TLM)resistance measurement of metallic nanowires.

The electric field and equipotential simulations of a electrostatic nanowire structure have been carried out using ELECNET, an electrical field simulation tool from Infolytica[89]. Although this software can be used extensively for simulating electric field of a capacitor model with metal and dielectric interfaces, metal in this software is often assumed as perfect conductors where the elec-

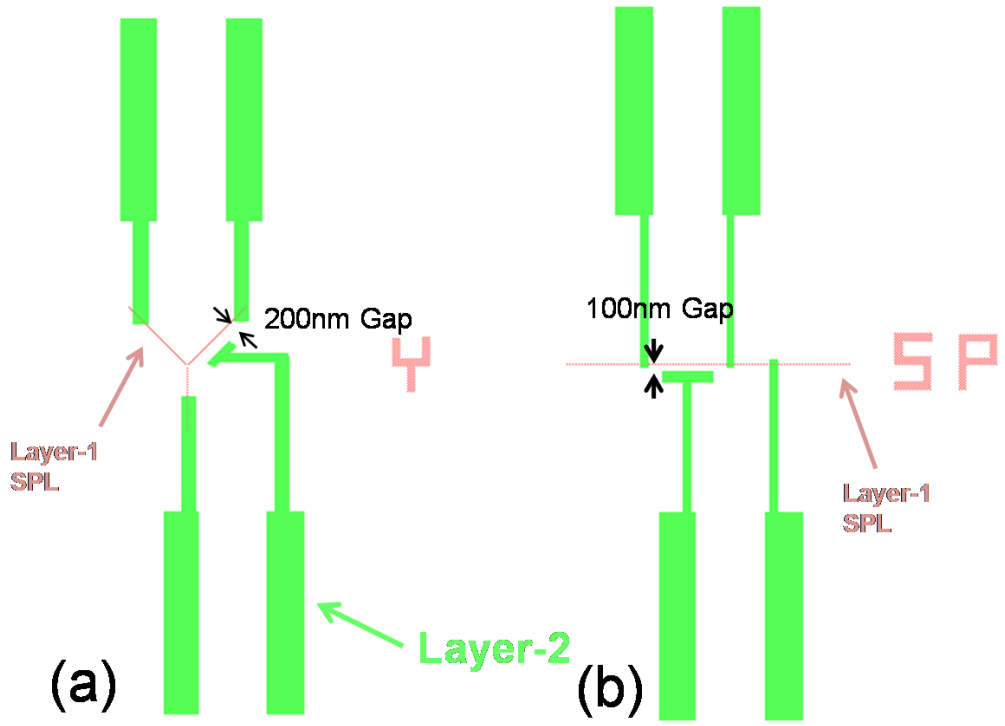


Figure 4.6: GDS-II design for (a) Y-branch nanowire transistor and (b) electrostatic metallic nanowire transistor.

tric field at any point within the metal is always zero. This simulation tool can be used for the approximation of the gate electric field coverage and distribution in our nanowire structures. Figure 4.7 shows the electric field distribution of $Ag/SiO_2/Ag$ interface in the double lateral gate model of electrostatic nanowire transistors. The simulations were carried out assuming a SiO_2 dielectric layer with isotropic resistivity of $10^{18}\Omega$m, isotropic permittivity of 3.9 at 25°C. Where the maximum Newton interactions[†] and polynomial order was set to 20 and 4 respectively[89]. The simulation of electric field distribution has allowed the approximation of electric field strength at any point along the surface of nanowire that was induced from a gate electrode. From the simulation result in Figure 4.8, an electric field up to $3.32 \times 10^8 V/m$ was exerted at the centre of nanowire/dielectric surface (at the point d=0) region normal to the gate, where a 70% cut-off of electric field was found to be 120nm across the surface. The distribution of electric field based on this model follows the classic electric field distribution profile, where a gate length greater than the nanowire length

[†]Newton tolerance was set to 1% with H-adaption option of 25% and 0.01% tolerance.

is desired for effective electric field penetration or depletion. However, in the EBL exposure process, the gate lengths were made shorter than the nanowires to accommodate the proximity effect caused by having a very long gate close to the nanowires.

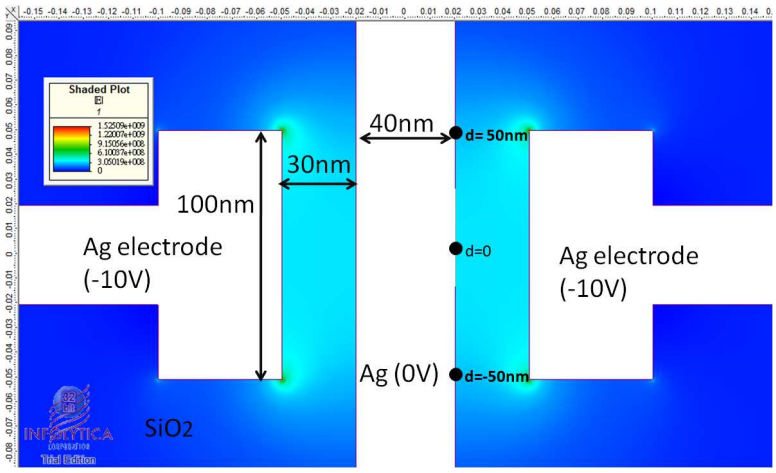


Figure 4.7: Electric field distribution of metallic nanowire in the presence of -10V gate voltages.

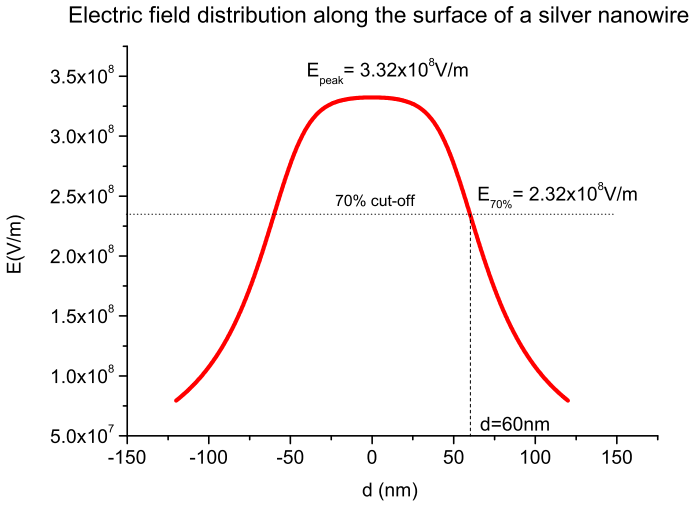


Figure 4.8: Induced surface electric field along the nanowire, where a peak electric field was exerted at the center region.

4.2.2 Pre-exposure alignments

Electrical measurements of nanowires and nanotransistor structures were conducted by probing onto the pre-defined gold contact pads. It is therefore critical to have high accuracy alignment between nanowire patterns and the underlying contact electrodes prior to E-beam exposures.

Write field alignments were carried out to the highest possible accuracy to prevent from any misalignment leading to electrical isolation during the characterisation process. During the electron beam optimisation process, the automatic calibrations of write field alignment in Raith were executed at least five times until the most satisfactory result were obtained. The typical stitching error after a write field alignment process for a Raith-150 system exposed at 10KeV is found to be around 30nm[75].

After the write field alignment and angle correction alignment, the three point alignment was performed based on three regions with known coordinates relative to the pre-defined contact pad structures. This allows very high accuracy of overlay for E-beam exposed pattern to contact electrode pads. Figure 4.9 shows the three point alignment coordinates for overlaying E-beam defined structures for various types of contact electrode patterns used in this work. These three points were normally aligned at the 2400X magnification, the same magnification used in Raith-150 under 25μm write field size to prevent alignment errors that were likely to occur at different magnifications. Figure 4.10 shows an example of high precision overlay between gold contact electrodes and EBL exposed PMMA pattern after three point alignment process. Resist and exposure details are: 90nm thick 2.5% HMW (996K) PMMA using 10KeV, 30μm aperture, 188pA E-beam current, and 25μm write field. One micron thick Si_3N_4 coated silicon wafer was used as the insulating substrate.

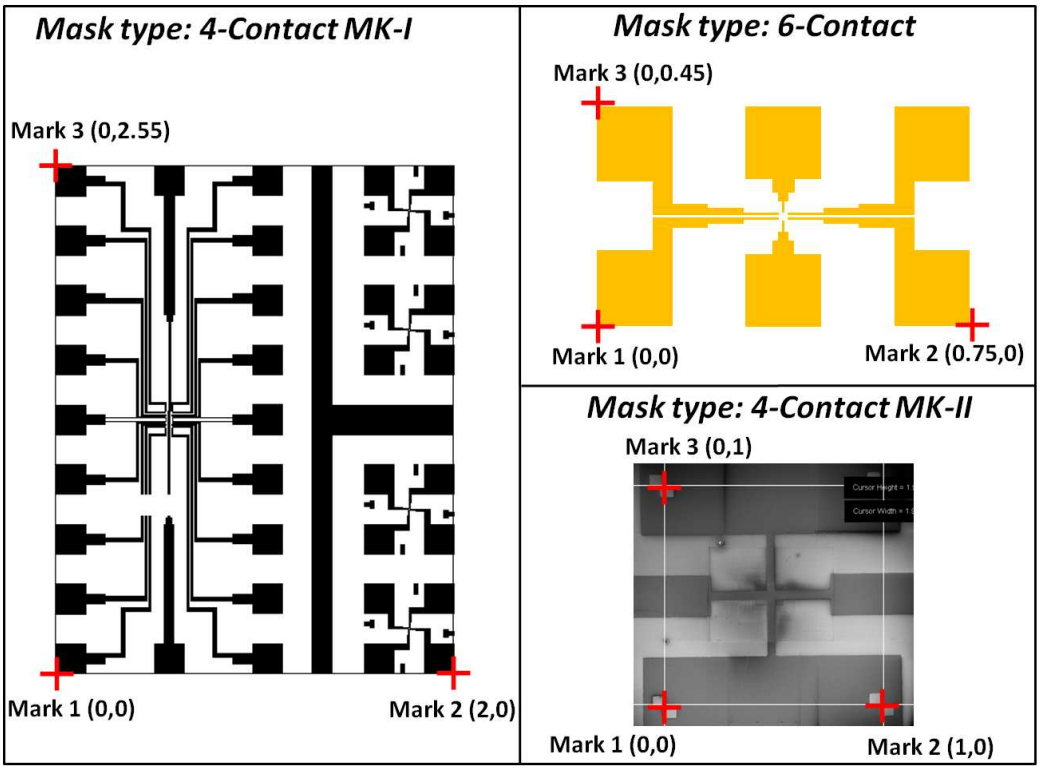


Figure 4.9: Three point alignment coordinates (units in millimeter)for each types of contact pad patterns.

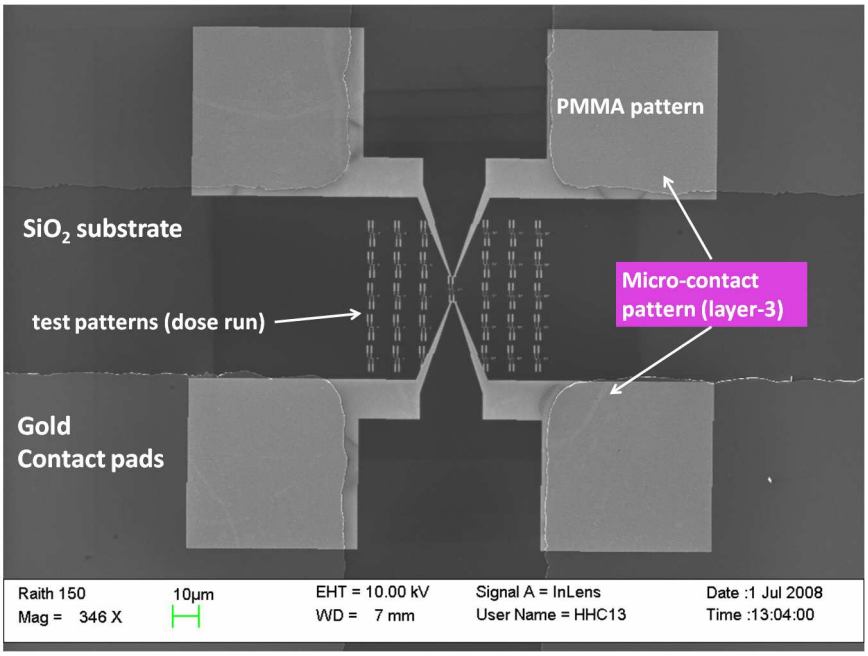


Figure 4.10: SEM image showing precise alignment of EBL patterned PMMA feature overlayed on gold contact electrodes. The bright regions are the exposed areas.

4.2.3 PMMA parameters

Among all types of E-beam sensitive resist, PMMA, a positive resist, has been the most widely used and studied. In this study, PMMA has been chosen as the most suitable electron sensitive resist for nanostructure pattern transfer due to its uniform resist coating, high resolution and high contrast for EBL exposures, long shelf life, and good adhesion to most substrates. In terms of exposure parameters, the clearing dose[‡] for electron sensitive resist depends mainly on beam energy and the resist material, where it remains independent to resist thickness.

For the fabrication, PMMA solutions prepared from 996K high molecular weight (HMW) and 120K low molecular weight (LMW) have been used. These includes 2.5%wt HMW PMMA with thickness ranging from 65nm to 100nm (996K molecular weight in chlorobenzene, spun at 4000rpm to 2500rpm for 1 minute), and 4%wt LMW PMMA (120K molecular weight in xylene, spun at 4000rpm for 1 minute, to produce a 120nm thick layer). The developments of exposed PMMA were carried out in Methyl-isobutyl-ketone (MIBK) in IPA (3:1) at 23°C for 31s, followed by rinsing in IPA and drying with N_2 gas.

In our previous experiments[65][12], EBL processes involve the use of Bi-layer PMMA stacking has been utilised to create an undercut profile suitable for lift-off of metals . During the preparation of bi-layer PMMA process, 4%wt 120K-LMW PMMA was spun onto the substrate at 4000rpm for 1min, followed by a pre-exposure bake at 185 °C for 30min and a second layer spincoating of 2.5%wt 996K-HMW PMMA at 4000rpm for 1min with a final pre-bake at 185 °C for 30min. The total thickness for the bi-layer PMMA was found to be around 200nm using DEKTEK 150 stylus system.

However, experiments based on E-beam exposure and lift-off using Bilayer PMMA have revealed low yields on achieving metal nanowire with linewidth less than 50nm. From experimental work, for highest resolution patterning, thinner PMMA layer with higher molecular weight is desired as it gives higher contrast between exposed/unexposed region during the development process [90][91]. Although the use of very thin (<30nm) PMMA layer can be utilised

[‡]The dose required to expose patterns with exact dimensions in the design.

to achieve very high resolution patterning, it was found to be not suitable for lift-off based metallisation processes. As a result, for the highest resolution pattern, PMMA with thicknesses of 65nm and 100nm were chosen for samples metallised with thermal and electron beam evaporation respectively.

Figure 4.11 shows the experimental data obtained for average area dose found to exposure PMMA under different acceleration voltages. In order to obtain the area clearing dose for each of the acceleration voltages, a 200nm wide, 10μm long rectangle pattern has been used as the test pattern. The exposures in EBL were carried out with same aperture size of 30μm and step-size of 12nm. The samples were then developed in MiBk:IPA (3:1) solution for 31s at 23°C and SEM images of the resist profiles were taken at 15,000X of magnification to examine for the clearing dose values. Error bars with 10% errors have been included in this graph and the fitted line indicates good linearity of the relationship between dose and voltage.

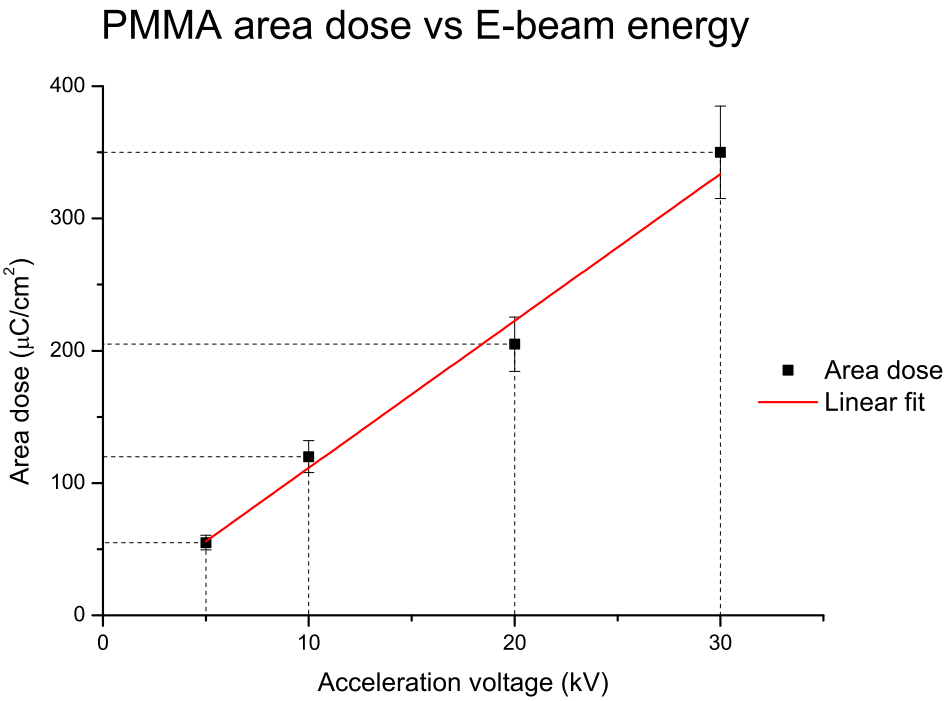


Figure 4.11: Experimental result of PMMA clearing area dose versus acceleration voltages.

4.2.3.1 Single pixel line exposure

Single pixel line exposure in EBL has been employed to deliver the smallest features on PMMA. The optimum dose required has been experimented on various exposure voltages ranging from 5kV to 30kV. In terms of determining clearing dose for single pixel lines, the dose required for continuous metal nanowires with smallest dimensions after lift-off process were averaged. The clearing dose required for single pixel lines were found to be both substrate and GDS-II structure dependent. Figure 4.12 shows the relationship for clearing dose of a four-point nanowire resistance measurement setup and the beam energy for 65nm thick, 996K 2.5%wt PMMA on SiO_2 substrate. For the highest resolution PMMA exposure on insulating substrate, the optimised parameters for EBL process were found to be: Acceleration voltage of 10KeV, 10μm aperture, 25μ write field, and beam current of 25pA.

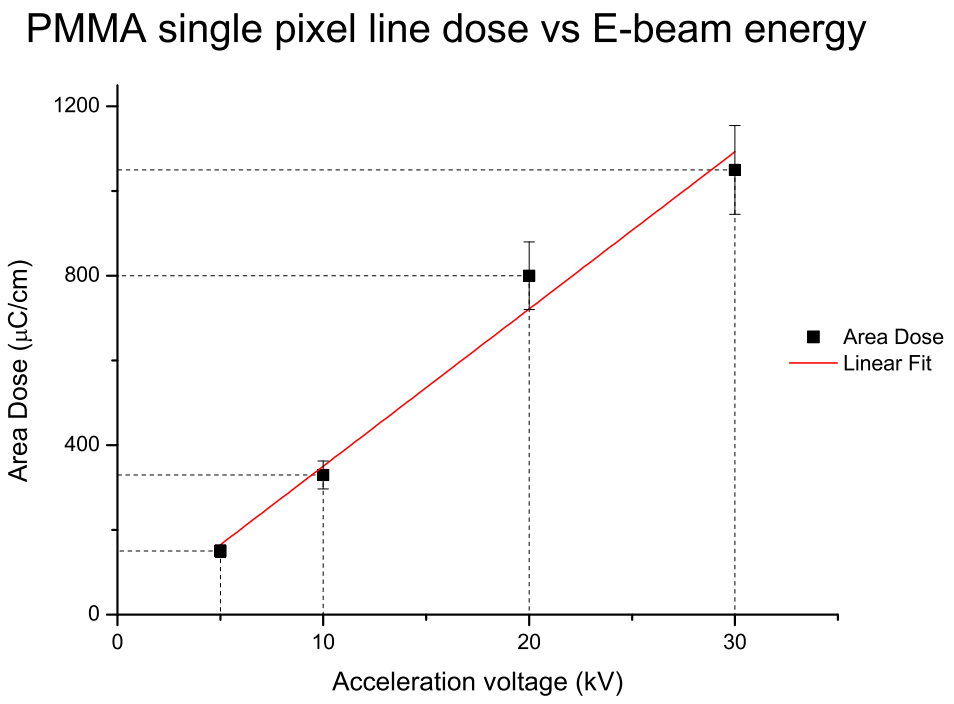


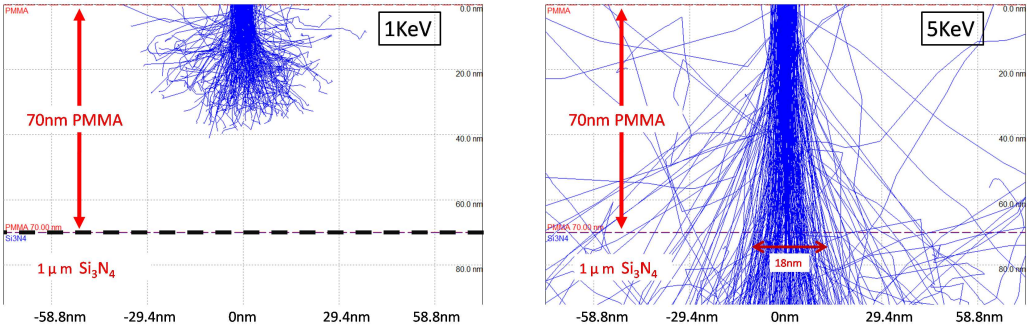
Figure 4.12: Experimental result of average PMMA single pixel line dose versus acceleration voltages (with 10% error bars).

4.2.4 Monte carlo simulation

In order to define patterns with the smallest possible nanowire width and gap structure using Raith-150 EBL system, exposures using various beam energies were simulated in CASINO v2.42. This software is dedicated for the Monte Carlo simulation of electron trajectories in any solids. In the simulation, the trajectories of both forward and backward scattered electrons in PMMA and Si_3N_4 substrate were simulated in a 5000 electrons model, with an average beam radius of 9nm, the typical dimension in our study.

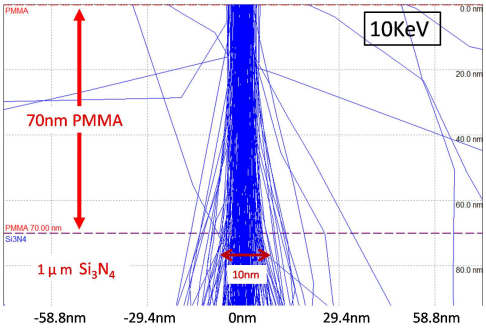
Figure 4.13 displays the simulated result for electron/PMMA/substrate interaction with E-beam exposure ranging from 1KeV to 30KeV. For voltages less than 5KeV, although the spread of backscattered electrons reflected from the substrate to the surface of PMMA is at the minimum, the spread of forward-scattered electron is relatively wide, indicating a poorer resolution of E-beam exposure for this condition. For voltages greater than 20KeV, although both the spread of backscattered and forward scattered electrons are smaller, experimental results have indicated severe charging effect and very poor secondary electron emission rate that would result in poor beam focusing, astigmatism and alignment adjustments when patterning on insulating substrates.

Although the patterning resolution was not as good at low voltages as at high voltages, there are two advantages to writing at lower-acceleration voltages. These are reduced proximity effect and reduced exposure time [92]. As a result, an exposure voltage of 10KeV has been chosen to give high resolution, reduced surface charging and acceptable proximity effects for nanowire and nanotransistor patterns on PMMA on insulating substrates.

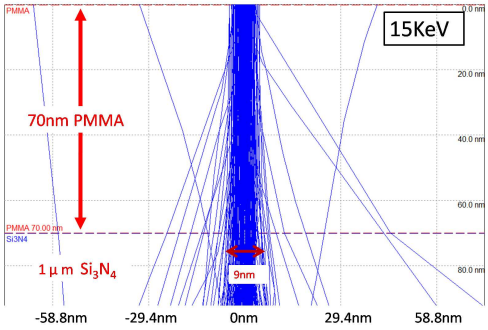


(a) 1KeV

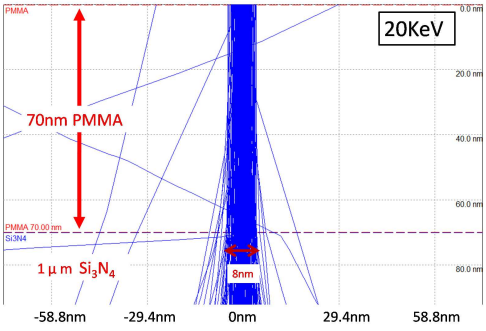
(b) 5KeV



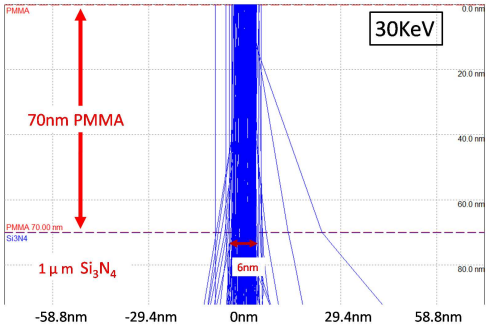
(c) 10KeV



(d) 15KeV



(e) 20KeV



(f) 30KeV

Figure 4.13: Monte Carlo simulation of electron PMMA-Si_3N_4 scattering interaction during E-beam exposure at different accelerating voltages, simulated in CASINO v2.42.

4.3 High resolution EBL patterning on insulating substrates

One of the main objectives of this study is to fabricate the smallest possible metallic nanowire for the gate effect measurement. This involves EBL exposure on insulating substrates like Si_3N_4, SiO_2, and quartz. A great effort has been spent on reducing the smallest line-width of EBL exposure on insulating substrates, while maintaining acceptable line edge roughness and fine-tuning metallisation process to obtain electrically conductive and continuous nanowires suitable for device characterisations. When it comes to EBL patterning on insulating substrates, trade-offs such as resolution and surface charging have to be made in order to deliver nanowires with smallest linewidths. Table 4.3 depicted the generalised resolution factors for EBL with different accelerating voltages [14][93]. This table was created based on both the experimental results of this work and some details from the basic resist theory presentation from Raith[14]. By optimising the writing strategy and E-beam parameters, 10KeV, 25pA beam current, and 10μm aperture were found to enable us to define and transfer wires as narrow as 12.5nm on insulating substrates.

Table 4.3: Relationship between beam energy, resolution and limitation[14].

Beam energy (keV)	1	10	30	100
Resolution	Low	medium	High	Highest
Proximity effect	Low	High	medium	Low
Surface charging	Low	Medium	High	Highest
Beam damage	Low	Medium	High	Highest
Secondary electron signal	High	Medium	Low	Lowest

4.3.1 Surface charging effect

In terms of direct EBL patterning on insulating substrates, the resolution and application are often limited by the surface charging effect. When an electron beam is scanned across the resist on a conducting substrate, the excess amount

of charges can be readily dissipated through the proper grounding of the sample, resulting in a neutral state of the substrate. However, for insulating substrates, the charges are instead trapped near the surface of the substrate, causing pattern distortion and beam deflection from the uneven surface potential of the resist[94][95].

The acceleration voltage used in the EBL process is related to surface charging. In this work, acceleration voltages higher than 10KeV were found to cause more charging than voltages below 10KeV, and for voltages as low as 3KeV, the surface charging can be greatly reduced. However, low energy beams were found to give poor resolution and linewidth, not suitable for defining sub 30nm structures on PMMA on insulating substrates. Figure 4.14 shows an example of pattern distortion caused by surface charging issues and electron beam bending during EBL process on 65nm thick PMMA resist deposited on 1μm Si_3N_4 coated Si substrate. This pattern was exposed on bare substrate at 20KeV with an aperture of 10μm at 25μm write field size.

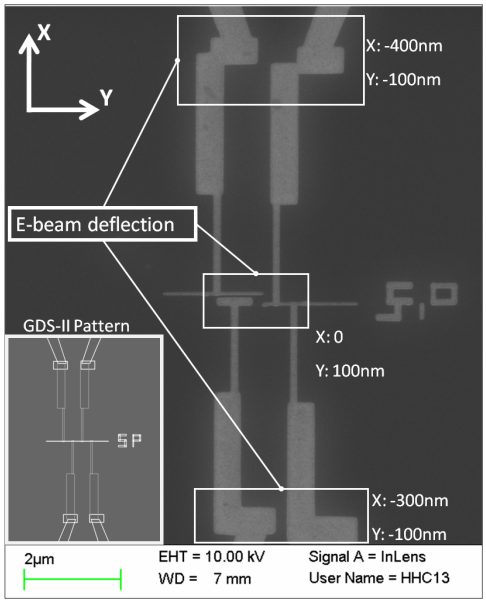


Figure 4.14: An example of severe beam deflection effect caused by direct patterning on insulating substrate. Insert shows a GDS-II pattern of a nanowire based structure designed for four-point measurement. Right hand side image shows the distorted resist pattern with regions shifted by up to -400nm and 100nm in X and Y direction, caused by the severe surface charging.

There are ways to minimise surface charging effects during EBL process, including the use of insulating membranes or substrates with thin insulator coatings, the use of metallic or conductive polymer layer above or below the resist[96][97], the use of conductive polymer resist[98], low voltage EBL process[92], and the variable pressure EBL process[99].

In this work, EBL exposures were performed on 200nm to 2μm thick Si_3N_4 and SiO_2 coated Si wafers. It has been found that for samples with 200nm thick insulating layers, although the surface charging issues were slightly reduced, pattern distortions due to charging were still observed.

Experiments on introducing charge dissipation layer at either above or underneath the PMMA layer have also been performed. Although EBL patterns with much less distortions were obtained with these approaches, charge dissipation layers have complicated the fabrication process upon removal by either RIE or wet etching, which often result in damaging the nanostructure features.

In order to reduce the amount of surface charges during EBL process, photolithographically defined contact pad patterns were made prior to the EBL process. These gold contact pads were designed in a way that they could cover most of the area of the substrate and the biggest pads were grounded through the metallic clips of the sample holder. By using samples with 200nm insulator coatings and pre-defined gold contact pads, the pattern distortion caused by surface charging was greatly reduced.

4.3.2 Proximity effect

In an EBL process, as electrons penetrate through resist material, they will be scattered by resist molecules and the substrate atoms as forward-scattered and back-scattered electrons. The majority of electrons will be forward-scattered inelastically with a smaller angle, while a smaller number of electrons are back-scattered elastically with larger angle[14]. As the forward scattered electrons slow down, secondary electrons with kinetic energies in a few eV are generated, resulting in unintentional resist exposure. The proximity effect is caused by the backscattered electrons having significantly higher energy that could expose resist further away from the beam incident point. The exposure contribution

from proximity effect depends intimately on number of factors, including:

- Pattern structures.
- Beam acceleration voltage.
- Resist material and thickness.
- Beam diameter.

The pattern layout can also cause unintentional proximity effects. By having highly packed features in a small area, the backscattered electrons of nearby structures induced by an electron beam can propagate and cause undesired exposure, resulting in pattern bridging. Another example for proximity effect can be given by having a large feature in close proximity to a very small feature, where the large feature receives more exposure than the smaller one, resulting in a proximity effect that affects the linewidth of the small structures[100]. As a result, for high resolution and small linewidth exposures, isolated single pixel line structures are normally employed. Figure 4.15 shows the example of proximity effect induced linewidth distortion, where the left and right branches of nanowire have linewidths of 23.34nm and 33.18nm respectively. The 10nm increase of linewidth of the right branch nanowire was caused by having a larger feature located 150nm apart. These structure was fabricated using single pixel line exposures for the nanowire branches at 10KeV, 24.5pA beam current, 10μm aperture, 25μm write field, and 16nm of step size on 1μm coated Si wafer.

The acceleration voltage also plays an important role during the exposure process. Figure 4.16 shows the effect of electrons scattering and their contributions toward resist exposure for acceleration voltages at 10KeV, 25KeV, and 50KeV. Due to the deep penetration of energetic electrons at higher voltages, the backscattering for electrons is located further from the resist, leading to less proximity effect caused by resist exposures from the backscattered electrons. In contrast to high voltage exposure, 10KeV suffered from the most severe proximity effects among these three acceleration voltages[8]. It was found that by employing very low acceleration voltage ($<$2KeV), the proximity effect can be greatly reduced due to low energy electrons that lose most of their energy in the resist[101].

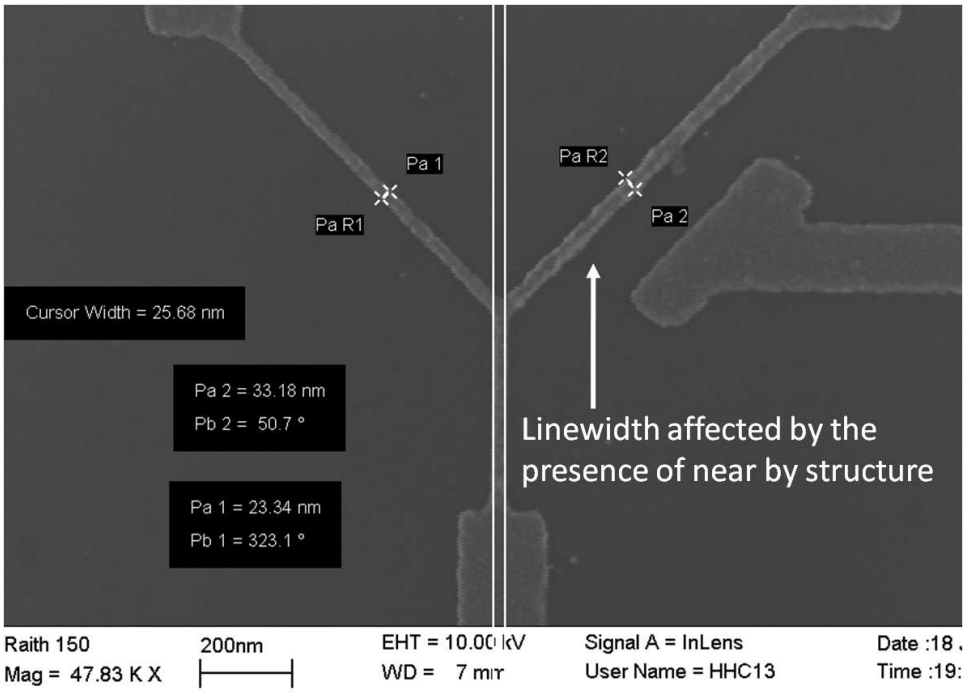


Figure 4.15: SEM image showing the linewidth variation caused by the proximity effect during exposure process.

Although the use of very high and very low acceleration voltage can reduce proximity effect during an EBL process, low energy beam have poorer performance in beam diameter[73], causing beam broadening and result in larger linewidths. For acceleration voltage as high as 30KeV, experiments were performed in Raith-150re on insulating substrate, 30KeV was found extremely difficult to perform proper beam optimisation process, and at the meantime, result in severe charging effect. As a result, 10KeV was chosen as the acceleration voltage for the fabrication of nanowire devices in this work. The thickness of resist was also found to affect the proximity effect. Figure 4.17 shows an SEM image of a nanotransistor pattern exposed on a 250nm Bi-layer PMMA coated Si_3N_4 substrate using 10KeV, 30μm aperture, 181pA beam current, and 25μm write field size. Insert shows structure design in L-edit in GDS-II format. From the SEM image, it has shown that the width of channel and the gap between gate and channel have suffered from severe proximity effect, resulting in increased channel width (from 50nm to 160nm) and decreased gap width (from 100nm to 50nm). By comparing this result with exposure result of thin (60nm) PMMA in Figure 4.15, the proximity effects for thin resist exposure were less observed.

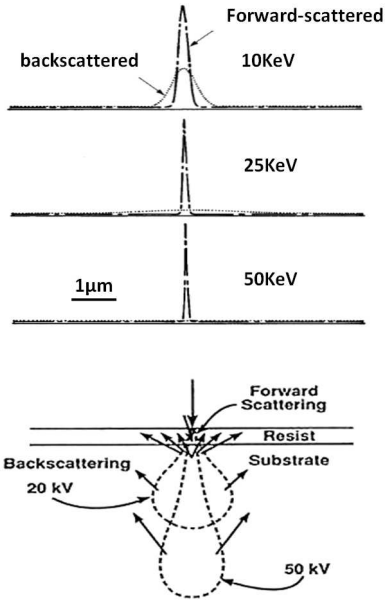


Figure 4.16: Electron, resist, and substrate interaction under different acceleration voltages, adapted from [8].

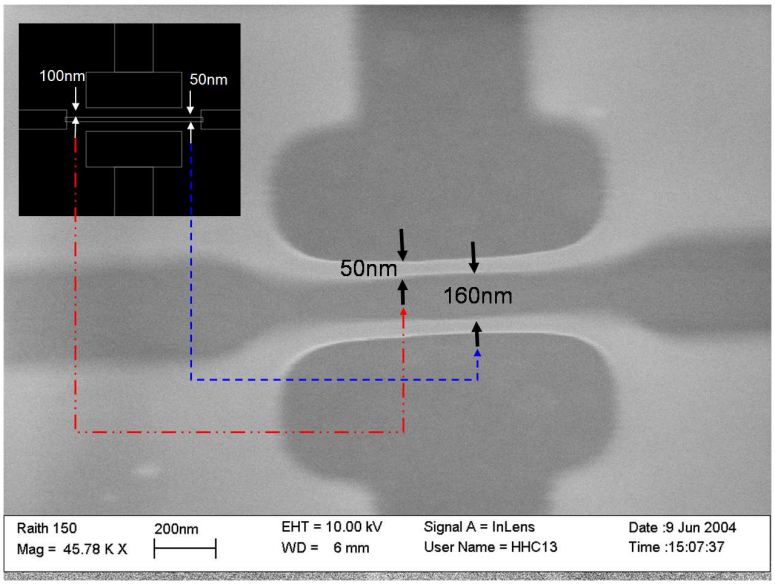


Figure 4.17: Insert shows the GDS-II pattern containing the design of a nanowire based transistor structure. In the main Figure, grey areas are PMMA pattern affected by severe proximity effect between nearby structures.

4.3.3 High resolution exposure parameters

In order to deliver the finest nanowire features on insulating substrates, the optimised exposure parameters was determined experimentally based on numerous factors. Figure 4.18 summarises these parameters based on the experimental data obtained in exploring the highest resolution exposures on insulating substrates. In this table we have only listed parameters that were considered to have significant influences on the linewidth and resolution of the EBL process. From the table, beam voltages were most significant to the surface charging issue, and the pattern layout and exposure techniques were found close related to the proximity effects. In terms of EBL resolution, both the write field size, and PMMA thickness can contribute to the linewidths of exposed patterns. A great effort was spent on the optimising of exposure and metallisation parameters in this study, allowing metallic nanowires as small as 12.5nm diameter to be fabricated.

EBL parameters and exposure resolution on insulating substrates

● Significant ◎ Medium ○ Minor △ can be neglected	Limitations		Resolution	
	Proximity effect	Surface charging	Throughput	Linewidth
Beam voltage	○	●	◎	◎
Dose	△	△	△	●
Pattern layout	●	△	○	◎
Step size	△	△	○	◎
Aperture	△	○	◎	◎
Write field	△	△	●	○
PMMA thickness	○	△	△	●

Figure 4.18: Summary of the significance of EBL exposure parameters for highest resolution patterning on insulating substrate using PMMA. This table was created based on experimental results obtained in this study.

For acceleration voltage in the range between 500eV to 30KeV, the surface charging effect was found most significant for beam voltages greater 20KeV.

Therefore a 10KeV was chosen as the acceleration voltage for high resolution exposures due to the reduced charging effects. These effects can cause strong beam deflection and scattering that made beam optimisation process difficult to perform, resulting in poor linewidth and contrast during the development process. For single pixel line exposure, the minimum linewidth depends closely on the pattern layout and dose used due to the proximity effects and exposure conditions. As a result, the dose required for the exposure of each type of nanowire patterns must be determined individually.

Figure 4.19 shows the effect of aperture and dose on minimum single pixel line-width obtained for nanowire structures fabricated on insulating substrate after metal lift-off. This chart contains 50 samples of nanowire features with minimum linewidths less than 80nm, while most of them are in the sub 50nm range. From this figure, it is clear that with 10μm aperture size, the linewidths are smaller than 30μm aperture ones mainly due to the smaller beam current (from 180pA to 24pA) used to expose the PMMA.

Figure 4.20 and Figure 4.21 illustrates the relationship between dose and wire size for sub 30nm nanowire structures on insulating substrates. In these figures, linewidths scale roughly linearly to the dose with reasonable fluctuations, as the linewidths of exposed feature depend on not only the aperture and dose, but also various factors such as development condition and beam conditions. By carefully optimising the beam conditions and the use of single pixel line dose, sub 13nm wide nanowire transistor channel structures have been successfully fabricated on insulating substrates, as shown in Figure 4.22. Figure 4.23 shows the smallest metallic nanowire structures fabricated in this work. This is to our knowledge, the smallest metal structure made on insulating substrate using Raith-150 EBL system, where a step size of 20nm has been used to improve the average linewidth during single pixel line exposure process. These devices were patterned with EBL using 10KeV, 10μm aperture, 300μC/cm dose with 100nm thick PMMA developed by ultrasonic agitation for 30 sec in MIBK:IPA(3:1) solution.

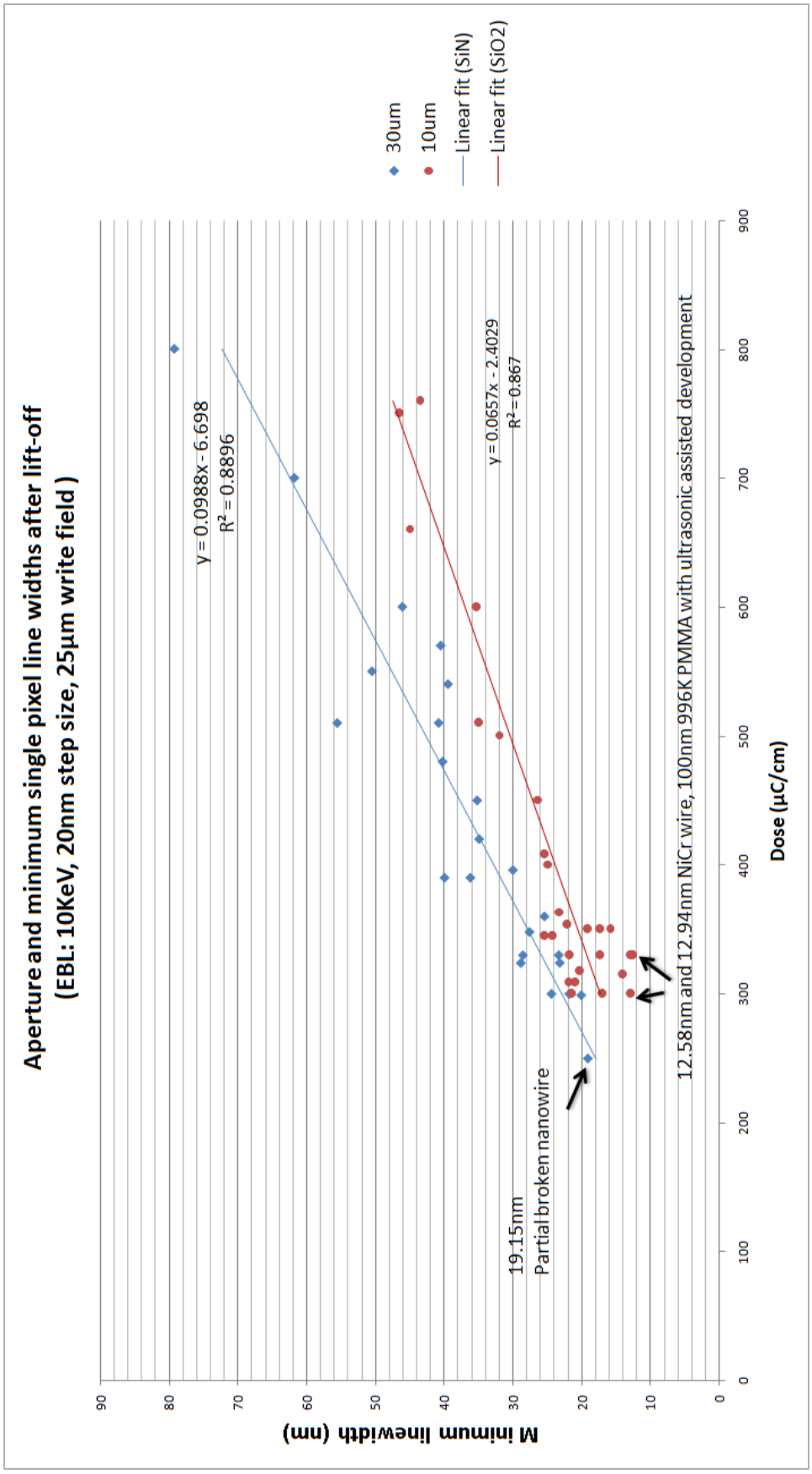


Figure 4.19: Aperture and minimum linewidth after lift-off.

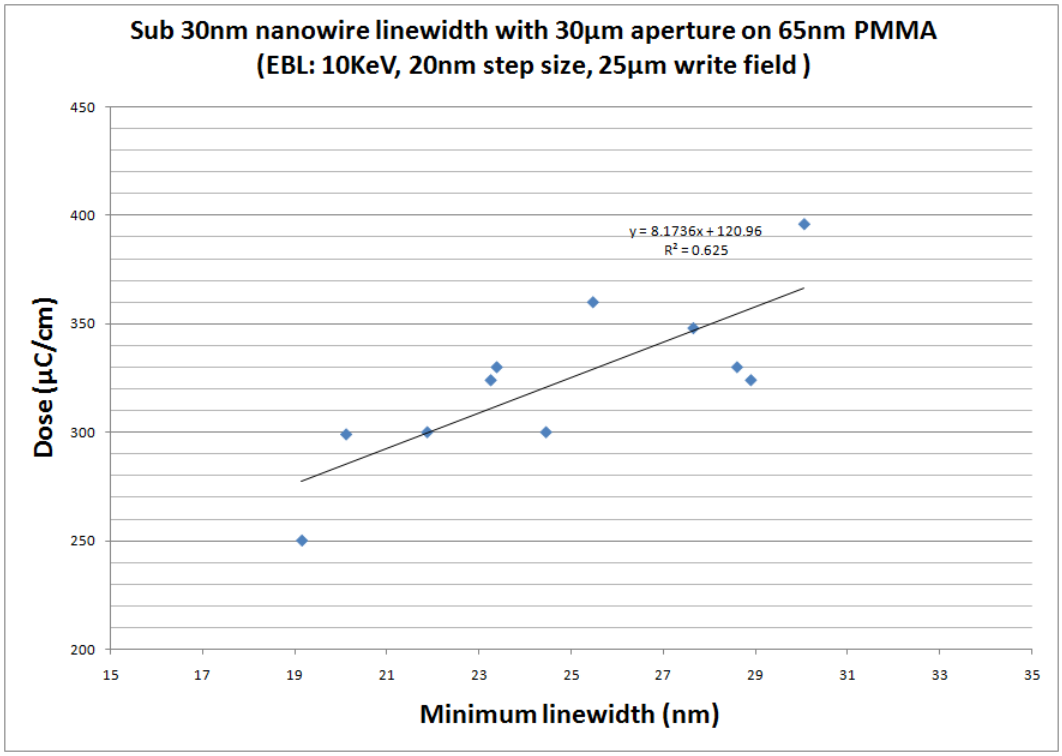


Figure 4.20: Sub 30nm wide nanowires obtained after lift-off using 30μm aperture.

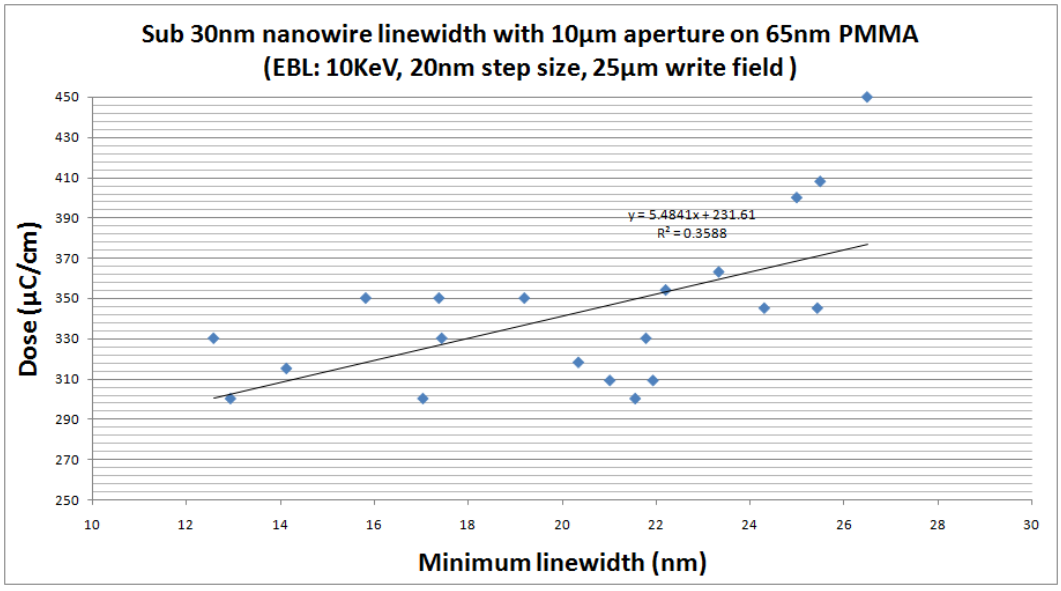


Figure 4.21: Sub 30nm wide nanowire obtained after lift-off using 10μm aperture.

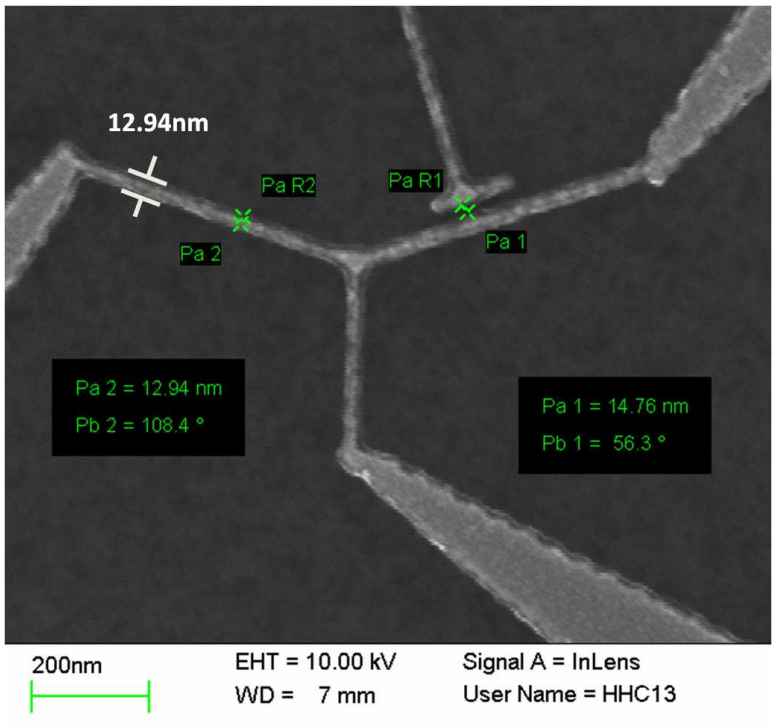


Figure 4.22: SEM image taken at 54,560X showing a Ag electrostatic nanowire based transistor structure on 1μm SiO_2 substrate with a nanowire width of 12.94nm.

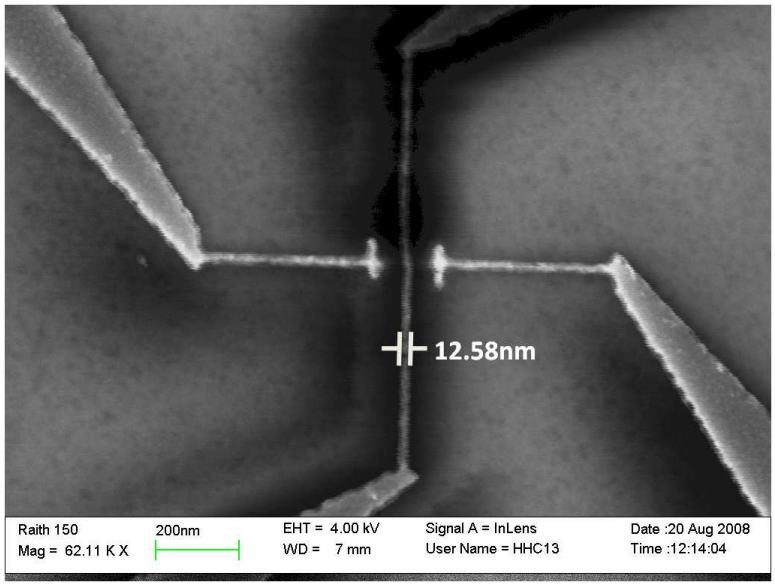


Figure 4.23: SEM image taken at 62,110X showing a NiCr nanowire and lateral gate structures with minimum linewidth of 12.58nm. This is the smallest metallic wire ever produced using Raith-150 on insulating substrates, where the detailed fabrication process can be found in Figure 4.3.

4.3.4 Development and metallisation

As previously mentioned, the resolution of a EBL pattern depends also on its development process. In terms of PMMA development, ultrasonic agitation during the development process has been reported to improve resist resolution[102]. Chen and Ahmed[103] stated that the intermolecular forces play a crucial role in the development process when the exposed regions approach the scale of the molecular size of PMMA, around 2nm. It is therefore, by developing resist with ultrasonic agitation, the energy of PMMA molecules can be raised, allowing them to dissolve more readily in the developer. From our study, although the ultrasonic assisted PMMA development did not show obvious improvement in nanowire linewidths for 65nm thick resist, it can be used to shorten the development time and improve resolution on high aspect ratio PMMA patterns[104]. However, when PMMA thickness was increased to 100nm, ultrasonic agitation of sample in MIBK developer has resulted in the creation of nanowires as small as 12.5nm after metal lift-off. We have also noticed the side effect of applying ultrasonic agitation during the development process, where large number of micrometer-size holes appeared on the PMMA surface by the sonicating process.

In this study, single layer of HMW PMMA 65nm thick has been used as the EBL resist for high resolution patterning and metal lift off when using normal development process, or 100nm thick resist with ultrasonic assisted development. In the metallisation process, metal liftoff normally requires high aspect ratio or undercut resist profile to prevent sidewall connections. N-Methyl-2-Pyrrolidone (NMP) or warm acetone was used for lifting off samples with sub 30nm metallic nanostructures on thin PMMA.

4.3.4.1 Cold development experiment

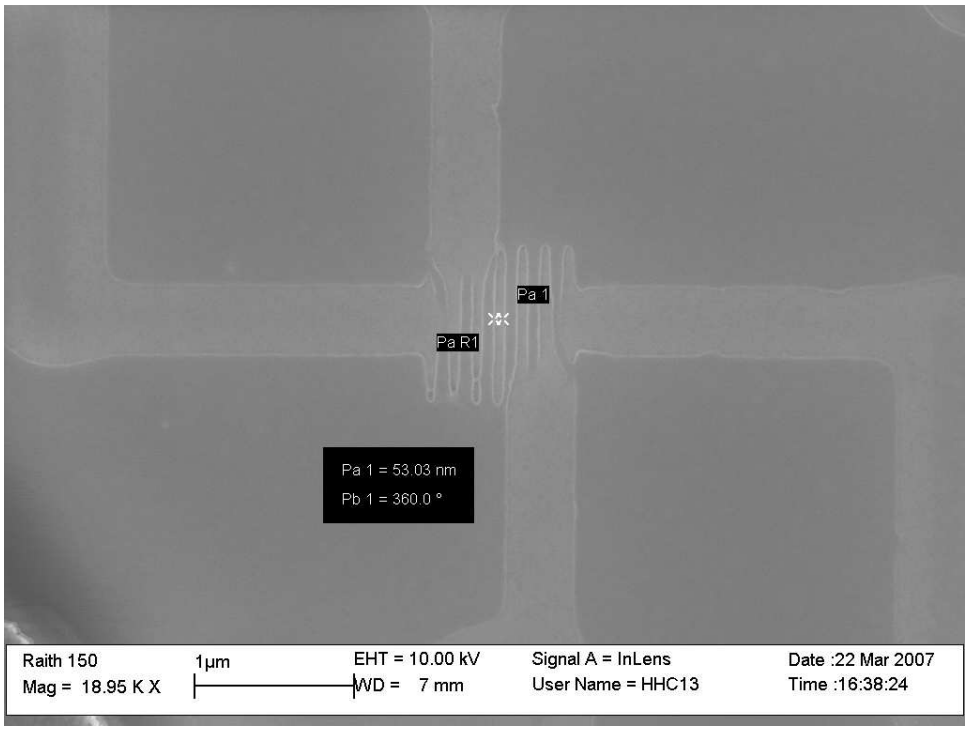
In 2005, Hu and Bernstein have demonstrated low temperature development of PMMA for sub 10nm EBL patterns. They claimed that by lowering the development temperature, the resolution and resist contrast can be improved [105][106]. Low temperature development experiments were tested in this study using similar EBL exposure parameters as in reference [105]. Figure 4.24 shows the E-

beam cold development result on samples exposed using 5KeV and write-field size of 30μm and 10μm respectively. The development temperature was maintained at 5°C using glycerol mixed water solution. Figure 4.25 shows the result of cold development for single pixel line patterns for samples exposed with 30KeV E-beam with dose of 1050μC/cm. A 10nm wide, 150nm pitch single pixel feature was obtained on a 2.5% HMW, 60nm thick PMMA. Although cold developed samples appeared to be smaller in dimension comparing to samples developed at 23°C, no nanowires were made after lift-off of 10nm of NiCr. The long developing time has made this process rather difficult to characterise and hence led to underdevelopment or excess resist residue that remained inside the fine trenches.

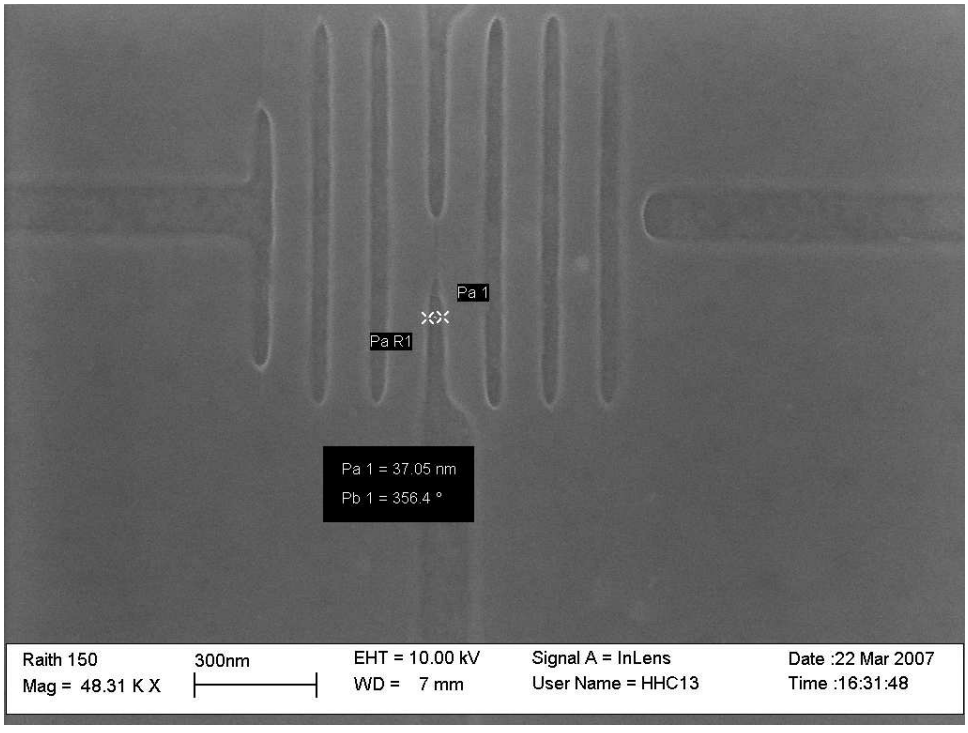
4.3.4.2 Metallisation requirements for lift-off on thin resists

Metal lift-off for a sub 20nm structure is challenging especially when it comes to lift-off of nanostructures using thin PMMA layers. Factors including step coverage of deposited materials, thickness of underlying contact pads that determine the minimum thickness required to cover and form uniform resist on the substrate, and the metal-substrate adhesion must be taken into account. In this study, RF sputtering, thermal evaporation and electron beam evaporation have been employed for the depositions of various types of metal thin films. Instead of using the Bi-layer PMMA system, a thin layer of high molecular weight PMMA has been used to improve the resolution of patterned resist. The ratio of the thickness of PMMA and the required metal thickness for thermal evaporation, electron beam evaporation, and RF sputtering were experimentally determined to be of 2, 5, and 10 respectively. For example, in order to perform lift-off of a 20nm thick metal structure, a 40nm thick of PMMA layer is required if thermal evaporation is used, whereas for E-beam evaporation and RF sputtered Ag film, 100nm and 200nm thick PMMA are required. These optimised ratios have allowed higher success rate for lift-off on thin PMMA structures. The minimum thickness of PMMA required for this project was 60nm as the thickness of predefined Au contact pads were around 50nm.

In our early work, acetone was used for PMMA lift off process. The samples

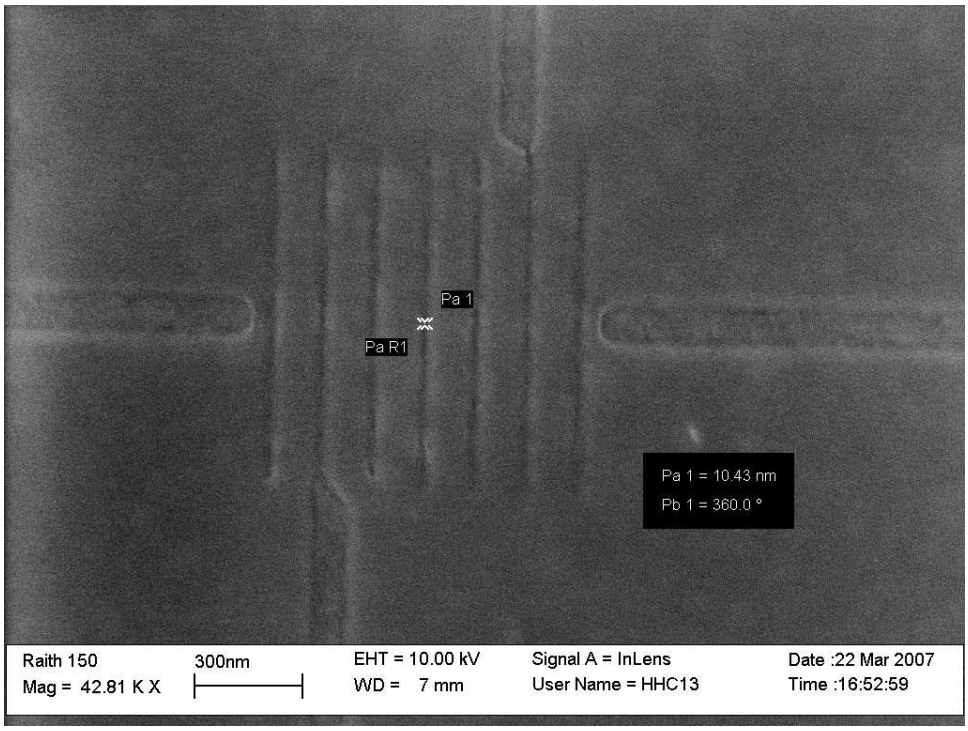


(a) sample patterned using 30μm aperture.

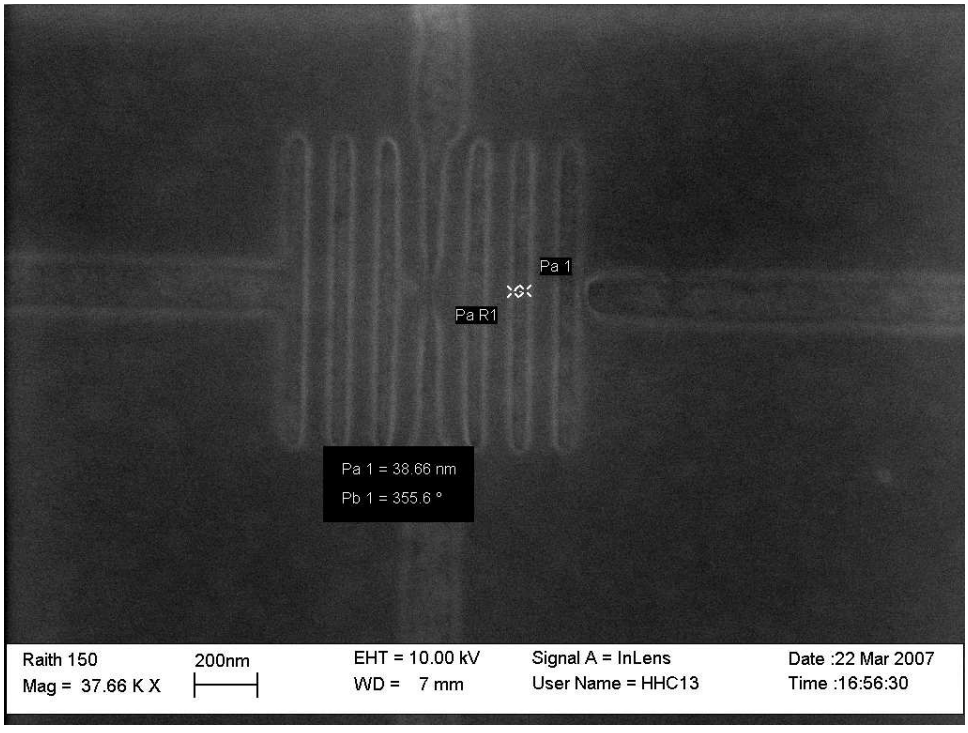


(b) sample patterned using 10μm aperture.

Figure 4.24: SEM images showing the result of 5°C 4 min Cold development for testing sample exposed at 5KeV using (a)30μm and (b)10μm aperture values.



(a) Sample developed using Cold development method.



(b) Sample developed at standard room temperature.

Figure 4.25: SEM images showing the results of 5°C 4 min Cold development for samples exposed at 30KeV, 10μm aperture.

were normally left in acetone for very long (8 hours) period to allow for complete lift-off of nanostructures. Due to the weak adhesion of thin and strained metal grains, ultrasonic agitation must be avoided. Our earlier results indicated that ultrasonic agitation during metal lift off result in a low yield in forming continuous metallic nanowires. Sometimes the nanowires would even be completely washed away because of the poor adhesion. In this work, N-Methyl-2-Pyrrolidone (NMP) has been used extensively for metal lift-off. The lift-off process were carried out at 65°C in NMP for approximately four hours on hotplate. NMP was found to be more effective in removing PMMA than acetone especially when heated.

4.4 Fabrication summary for EBL defined metallic nanostructures

The aim of this thesis is to develop the fabrication processes for implementing metallic nanowires structures that act similar to JFET drain and source channel and explore any transistor like operations. The narrowest nanowire channel was defined in EBL using the highest resolution parameters (10KeV, 10μm of aperture, 25pA of beam current, 20nm of step size and dose around 300μC/cm) for direct patterning on PMMA coated insulating substrates. Metallic nanowires have been used in various nanostructures in this work, including nanowires for two point, four point resistance measurements, transmission line measurement, and also, electrostatic nanowire transistor structures with lateral gates for gate effect measurements. Prior to any electrical measurements, the metallised nanostructures were normally inspected under the SEM for defects and linewidth analysis.

Figure 4.26 shows the summary of techniques applied and progress made in improving the EBL performance. A great effort has been spent on optimising and finding the process conditions to achieve conductive metallic nanowires with smallest cross sectional area. And to address the challenging issues involved in patterning gate structures as close as 20nm to the nanowire mainly by employing single pixel line exposure of isolated structures.

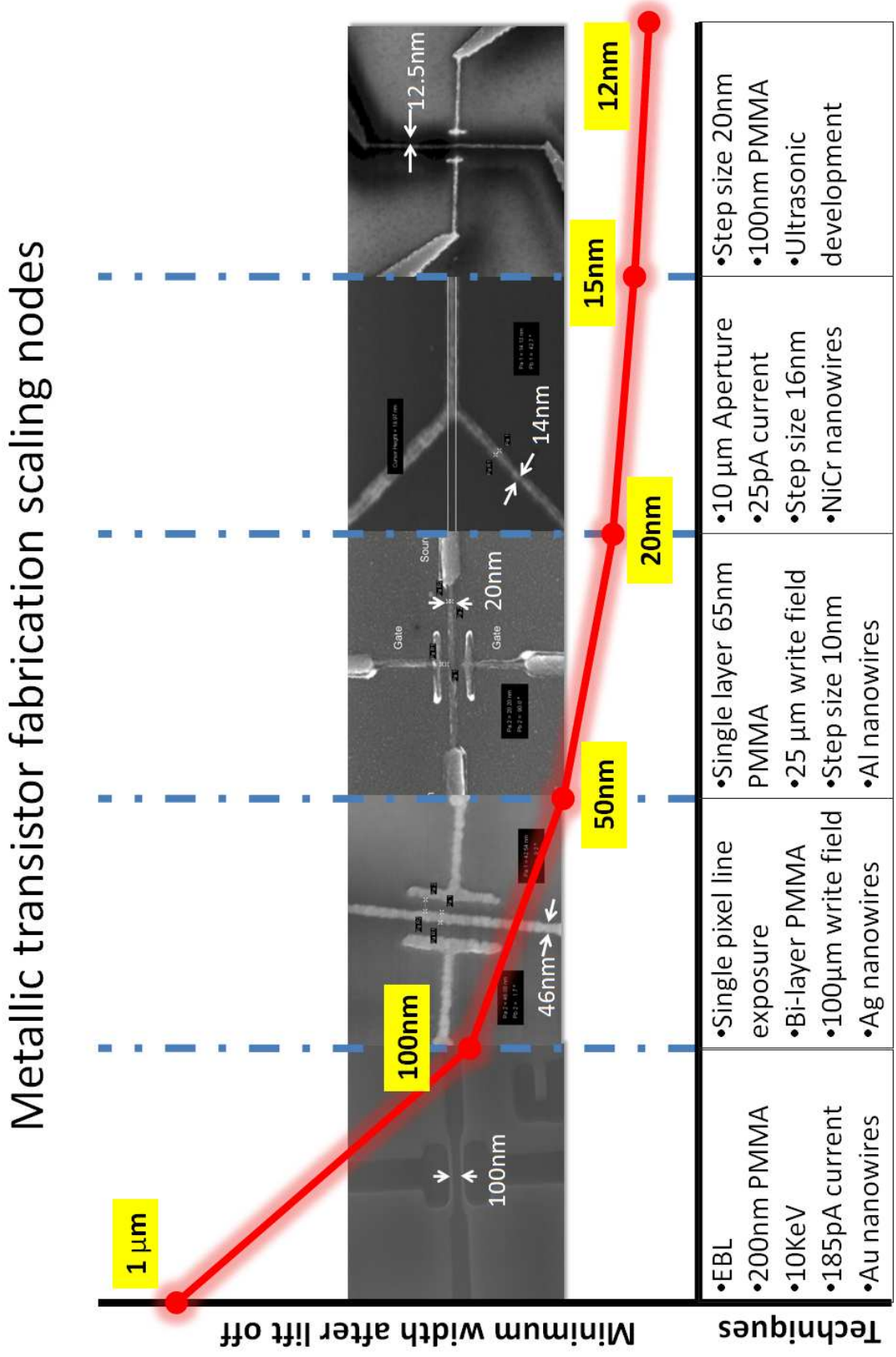


Figure 4.26: Advancement of improved linewidth for pattern transferring on insulating substrates using EBL.

4.5 Silver thin film transistor

As a requirement for making one of the dimensions of metallic nanowire few nanometers thick, thin silver films were used. The proposed structure utilises a top gate structure for studying gate effect on ultra thin metal films. Due to the poor quality of Ag deposited using thermal evaporation, RF and electron beam sputtered Ag has been employed for making very thin Ag film on SiO_2 substrates. It has been found that the minimum thickness required for Ag thin film to be conductive were around 15nm or 7nm, depending on deposition techniques (Electron beam evaporation or RF sputtering) used.[§].

10nm thick Ag thin film structures have been designed, fabricated, and characterised. The fabrication process can be summarised in Figure 4.27. First, a thin layer of high purity 99.999% Ag was RF sputtered on a SiO_2 coated Si substrate. It was followed by pattern transferring this thin film into wire structures (with typical dimension of 25μm by 4μm) using photolithography and wet etching. Where AZnLOF2020, a negative photoresist has been employed for photolithography process. An 1M $Fe(NO_3)_2$ solution was used as silver etchant. The time taken to etch 10nm Ag film was found to be around 5 seconds. Once Ag wires were fabricated, the contact electrodes and bonding pads were defined using photolithography and thermal evaporation, followed by lifting off in NMP at 65°C. The contact electrodes were designed in a way that, four point resistance measurements can be taken while the gate voltage is applied externally using Keithley 2400 sourcemeters. In order to align the contact electrodes onto the Ag thin film wires, various alignment marks have been designed for aligning each one of the four photomasks required for the fabrication process. Figure 4.28 shows an example of good alignment between photoresist pattern and the Ag thin film wire structure.

The samples were then electrically tested for conduction using HP4155A

[§]This was done experimentally using a multimeter that measured the resistances for various thickness of Ag layer deposited using E-beam evaporation and RF sputtering. For a conductive Ag film the measured resistances were ranging from few Ω to 20Ω on 10mm by 10mm test samples.

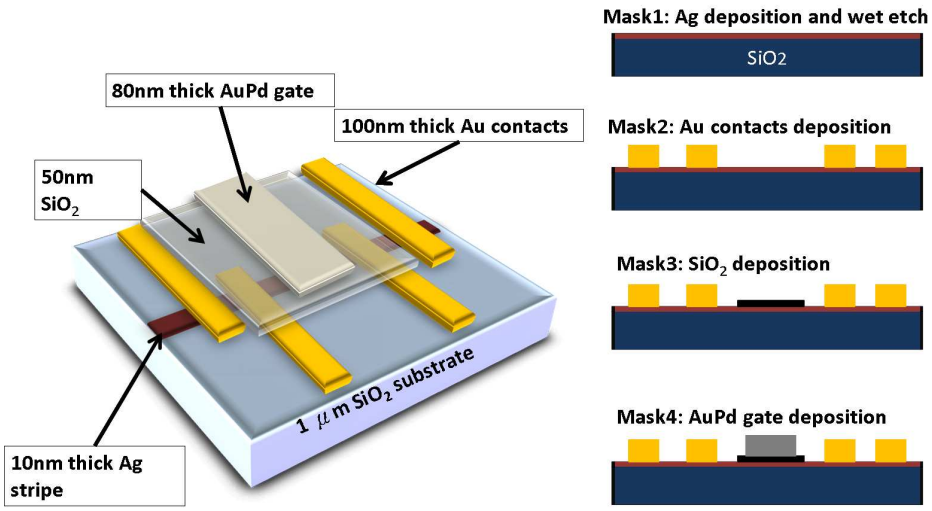


Figure 4.27: Left: Schematics of a Ag thin film transistor, featuring an nanowire with thickness as thin as few nanometers. Right: Fabrication process and photomasks required for Ag thin film transistor structures.

semiconductor parameter analyser after the creation of contact electrodes and bonding pads. The successful samples were then patterned in the mask aligner and RF sputtered with a 50nm layer of SiO_2 as gate dielectrics. Finally, gate electrodes and their bonding pads were created by another photolithography process, followed by E-beam evaporating of 50nm AuPd film and the lift-off process.

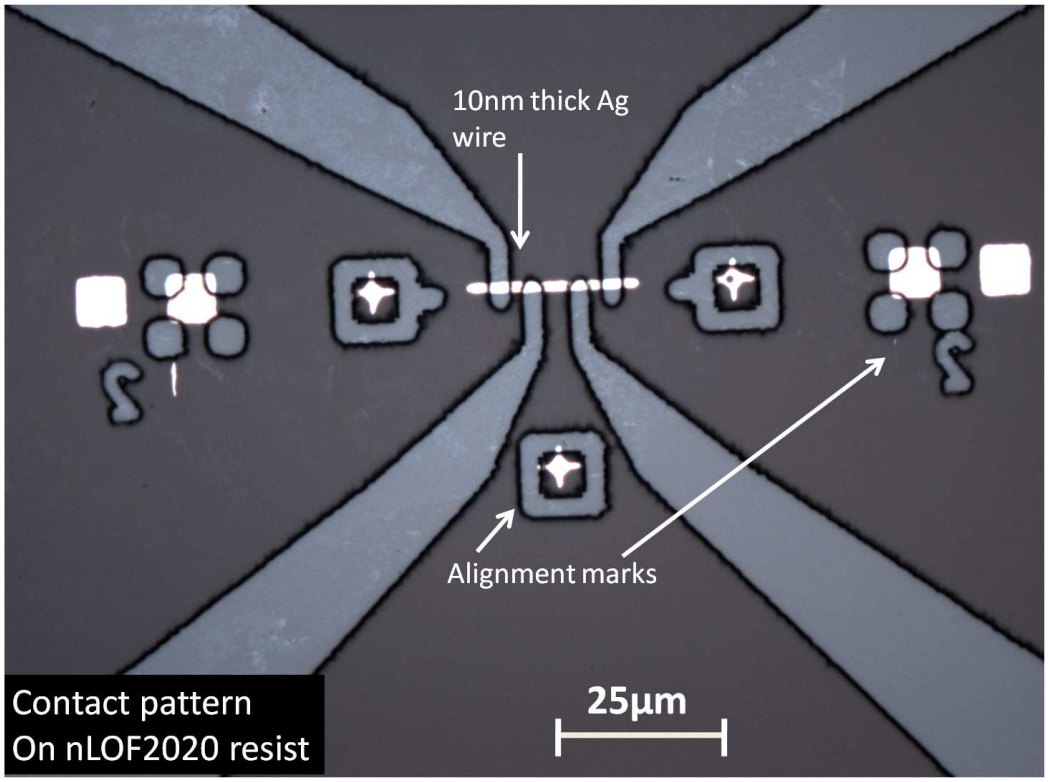


Figure 4.28: Image taken by optical microscope showing the alignment between Ag wires and contact electrodes patterns on AZnLOF2020 photoresist.

4.6 Summary and discussion

Thin metal nanowires can be fabricated using various approaches. Natelson[107] reported the fabrication of AuPd nanowire with 3nm in diameter by etching into a cleaved molecular beam epitaxy (MBE) grown substrate that acted as a template with atomic lateral definition. In their work they were able to conduct electrical measurement for nanowires greater than 5nm in diameter, indicating a maximum resistivity up to $3^{10}\Omega/m$ for 5nm wide AuPd wires. The use of this technique limits the fabricated structure to be wire only due to the geometry of MBE grown layer, not suitable for structures such as contacts or lateral gates. Other techniques such as AFM nanoscratching[108], or by employing chemical growth of metal nanowires[109] can be utilised to synthesise and fabricate metallic nanowire structures. However, the reported diameters are often larger than EBL fabricated ones and require extra steps to form contacts to these nanowire structures.

For the fabrication of metallic nanowires using EBL, Cumming[110] demonstrated the fabrication of 3nm NiCr nanowire on Si substrate by utilising the secondary electron exposure from the nearby 20nm wires over a gap formed by blanking a single pixel line for several pixels. This is to date the thinnest structure ever created using EBL in the world. However, this process is not feasible for repeatable and reliable fabrication due to the dependence of secondary electron scattering and the use of semiconducting substrates. In our study, we were more interested in developing an EBL process suitable for defining sub 20nm features onto PMMA coated insulating substrates. Joo[95] proposed the use of critical energy of EBL for direct patterning on insulating substrates to reduce charge induced pattern distortion. In their work 50nm features can be defined using acceleration voltage as low as 1.3 KeV. Although the dimensions of smallest features are almost four times larger than our best result, no charge dissipation layers were required.

In the development of nanowire structures, single pixel line exposure in EBL was found to give finest linewidths. Other factors like the development process, surface charging, and the choice of metals and their deposition process have their limits on the resolution. To suppress the surface charging, con-

tact electrodes and bonding pads structures were designed in way to cover a large portion of surface areas. By employing an accelerating voltage of 10KeV, 10μm aperture, 25pA beam current and 20nm of step size, we have successfully demonstrated the ability of delivering 12.5nm scale structures on insulating substrates using Raith 150. In fact, this is one of the smallest features defined on insulating substrates using this system. The use of ultrasonic assisted development has allowed us to reduce the linewidths size from 15nm scale to 12nm scale, and the reduced PMMA thickness was found to give finer width at a cost of poorer lift-off properties. Our fabrication process has demonstrated high yields for fabricating continuous and sub 20nm wide nanowire features.

The metallisation processes are crucial in forming continuous and conducting metal wires. In this work, we have studied thermal evaporation, electron beam evaporation and RF sputtering for depositions of Au, Ag, Al, NiCr, and AuPd metals. Thermal evaporation was found most suitable for lift-off process with sub 100nm thick PMMA and RF sputtering was found to give lowest resistivity and high quality coating for Ag thin films on SiO_2 substrates.

Hu[105] demonstrated the use of cold temperature (5°C) development for delivering sub 10nm features on PMMA, and Ocola[111] has reported (-4°C) degree development for 13nm features using Raith-150. In order to push our nanowire structures into sub 10nm dimension, the cold development tests were performed. These tests yielded rather poor development for our 60nm PMMA sample and we were not able to obtain good nanowire structures after metal lift-off.

Ag thin film structures have also been explored for the fabrication of ultra thin (sub 10nm) film for gate effect measurements. In this experiment we were able to deposit a conducting Ag layer as thin as 7nm thick using RF sputtering. However, due to the complicated processes and dielectric sputtering that yielded highly porous SiO_2 layers, the gate effect measurements of these structures were not successful. Nevertheless, we were able to study the electrical properties of such thin layers using four terminal measurements. These results will be presented in Chapter 6.

Chapter 5

Fabrication of Bismuth Structures

Previous chapter details the fabrication of metallic nanowire structures using EBL. Due to the resolution limits of EBL patterning on insulating substrates, we were only able to make metal nanowires as thin as 12.5nm in diameter, much larger than the typical screening length of metals. In order to explore the EFE measurements of metal, bismuth, a semimetal material with unique transport properties was employed.

Bismuth (Bi) is known to undergo a semimetal-to-semiconductor transition by size dependent quantum confinement[9]. It possess a typical screening radius of 40nm[112], much greater than that of conventional metals. This weak screening of bismuth is exceptionally suitable for implementing into metallic nanowire transistor structure with potential of more observable transistor operation. In fact, Bi nanowire has been recently demonstrated to possess gating effect suitable for field effect transistor applications[10].

The fabrication and electrical characterisation of Bi nanowires are extremely difficult due to its low melting point (271 °C), poor surface roughness of deposited film and thick native oxide coating[113]. Previous studies have explored the fabrication of Bi nanostructures by pressure injecting molten Bi gaseous into anodic alumina templates[114], by deposition of Bi nanoclusters[115], and by focused ion beam (FIB) milling of Bi thin films[116]. Due to the presence of thick oxide layer, these fabrication techniques often employ FIB systems for constructing ohmic contact structures to Bi nanowires.

For the first time, we have investigated the use of focused ion beam (FIB)

to fabricate Bi nanowire based structure for EFE measurements. For the fabrication of the proposed structure, 50nm of bismuth film was first thermally evaporated through EBL patterned PMMA windows onto SiO_2 substrates with pre-defined Au contact pads. It was followed by FIB milling of the thin film into Bi nanowire widths ranging from 30nm to 1μm using 30KeV Ga^+ ion beam in the FEI nanolab nova 200 FIB system.

During the development of FIB process, single-pixel-line ion beam blanking technique has been utilised to fabricated Bi nanowire 30nm in diameter on SiO_2 substrates. In order to form good ohmic contact to sub 50nm bismuth nanowires, a mill-and-fill process has been developed by employing FIB to sputter away the surface oxide of bismuth during the in-situ electron beam induced platinum nanowire contacts deposition. This chapter details the development, the fabrication and the ohmic contact formation for sub 50nm Bi nanowire structures using FIB systems.

5.1 Bismuth properties

Bismuth is a semimetal that has unique transport properties. It has drawn great attention soon after the demonstration of clear evidence of quantum confinement of bismuth by Ogrin, Lutskii, and Elinson in 1966[117]. The interesting thermoelectric and size dependent transport properties of bismuth have allowed researchers to observe and study the quantum effect of nano/atomic scale devices on relatively large diameter of Bi nanowires. This is mainly due to the small effective mass of carriers and the extremely long electrons mean free path of bismuth [118].

For bulk bismuth, the indirect valence band overlaps its conduction band by 38meV at 77K. As the dimensions of Bi nanowire decreases, the energy overlap decreases. As the nanowire width has reached its critical width of 52nm, an energy bandgap has been observed at 77K [119].

Sun [120] and Choi[121] described the effect of quantum confinement that led to bandgap opening for bismuth nanowire with width of a by the equation:

$$\triangle = \triangle_{bulk} + \frac{\pi^2 h^2}{2a^2 m_y^{e,h}} + \frac{\pi^2 h^2}{2a^2 m_z^{e,h}} \tag{5.1}$$

where $\triangle_{bulk}$ and $\triangle$ are the energy gap of bismuth. Also in Equation 5.1, h is Planck's constant, a describes the width of a square Bi nanowire with a^2 in cross section, $m_y^{e,h}$ and $m_z^{e,h}$ represent the effective mass of carriers in the lateral and current flow direction along the nanowire. The bandgap opening can be derived from the semimetal ($\triangle_{bulk} = -38meV$) to semiconducting transition ($\triangle > 0$) with a critical wire width of 52.1nm[120].

Although the semimetal to semiconductor transition of bismuth was predicted nearly 40 years ago, it has not been proven experimentally until the past few years due to the fabrication difficulties involved and the challenges in the characterisation of bismuth nanowires. Figure 5.1 shows the resistance plot versus temperature for Bi nanowires in various diameters[9]. From it one can clearly see a metallic behaviour (increase of resistance with increase of temperature) for Bi nanowires with diameter greater than 55nm and a semiconductor behaviour (decrease of resistance with increase of temperature) for sub 50nm

nanowires.

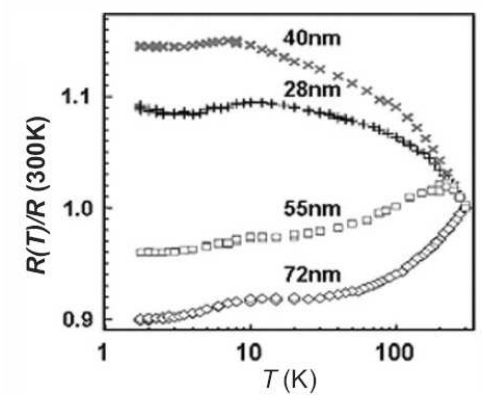


Figure 5.1: Size dependent semimetal to semiconductor transition, adapted from [9].

In addition, due to the highly anisotropic Fermi wavelength of bismuth, very weak screening of electrical field is expected. The screening radius for bulk bismuth is around 40nm, whereas for most conventional metals it is around a few angstroms[112][9]. This weak screening of Bi material would lead to a complete electric field penetration into a thin semiconducting Bi nanowire, resulting in the possibility of complete electron depletion inside the nanowire in the presence of gate induced field[10]. Lee[10] has successfully demonstrated the gate effect of bismuth nanowires with a diameter of 120nm. In fact, from their experimental result, the material can be turned into a pure hole or pure electron material by supplying a gate voltage of <-35V and >+35V respectively, as shown in Figure 5.2.

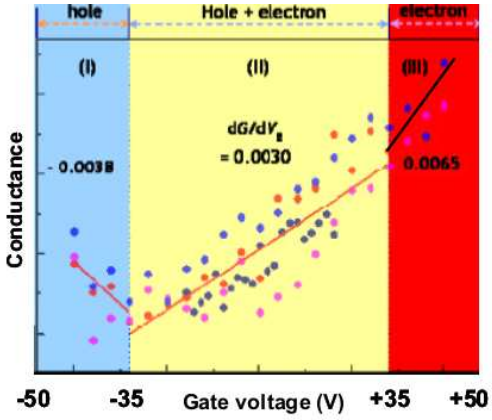
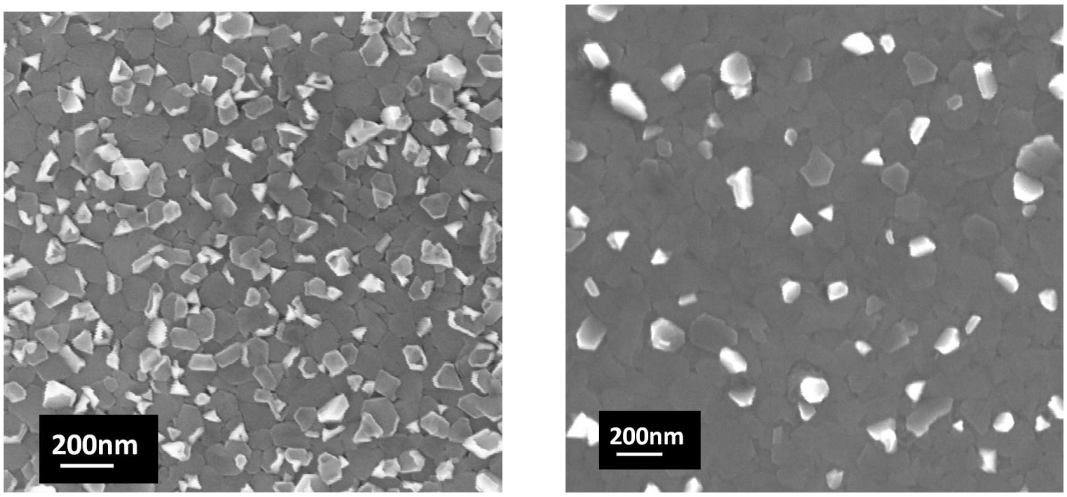


Figure 5.2: 4 point conductance versus gate voltage for 120nm wide Bi nanowire , adopted from [10].

5.2 Fabrication Process

5.2.1 Bismuth film deposition

For the fabrication of nanoscale bismuth structures, high purity Bi (99.999% purity) was deposited on insulating substrates such as SiO_2 and quartz using thermal evaporation and electron beam evaporation. Due to the low melting point of bismuth 271°C, a dedicated evaporation system for Bi has to be used to avoid cross-contamination for other depositions. In the experiment, 50nm thick bismuth films were evaporated at 10^{-5}Torr. It has been found that once the current start to flow through the Bi crucible, the material melts rapidly and the charge inside the crucible may disappear in just few seconds if the current is set too high. However, by slowly ramping up and keeping the current under control (81A in our case), 50nm Bi thin film can be successfully deposited at a rate of $1\mathring{A}/s$. A Bi film thickness of 50nm has been chosen to withstand the oxide removal process, and also to achieve a reasonable milling rate[122]. Figure 5.3 shows the SEM images of Bi films deposited on Si and SiO_2 substrates using thermal evaporation. It is noted that the grain size of bismuth on the Si (74nm) substrate is about 30% smaller than the one on the SiO_2 substrate (108nm).



(a) 50nm of Bi thin film evaporated on Si substrate.

(b) 50nm of Bi thin film evaporated on SiO_2 substrate.

Figure 5.3: SEM images of thermally evaporated Bi films on Si and SiO_2 substrates, where the average grain size on Si is around 30% smaller than on SiO_2 substrate.

To further examine the surface morphology of deposited films, AFM has been employed. Figure 5.4 is an AFM image taken using NSC-11 AFM tip with tapping mode, showing 50nm of bismuth film in 3D. These AFM images indicated the presence of large size bismuth grains at the scale of 70-200nm. From other research work, Ramadan[123] has observed the growth of columnar like granular structures with their sizes (100nm) in direct proportion to the film thickness for thermally evaporated bismuth on glass. In addition, Kumari[124] reported high quality poly-crystalline Bi film with grain size of 128nm on Si using thermal evaporation at $1\mathring{A}/s$, around 40% larger than our result using similar setup, where a higher pressure 10^{-6} Torr was used.

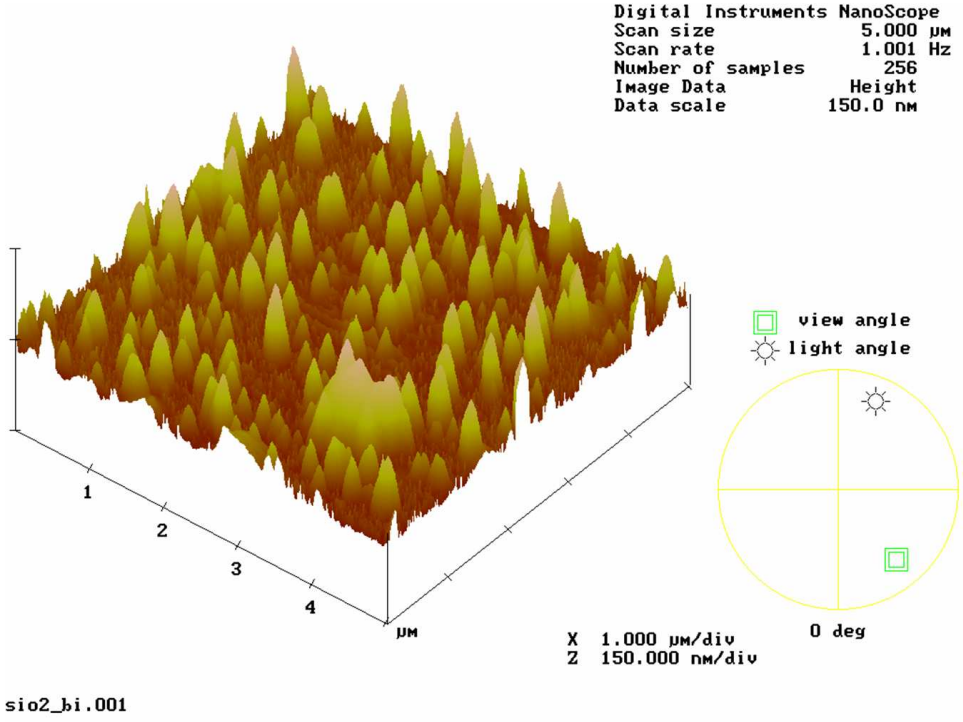


Figure 5.4: AFM image of bismuth film on SiO_2 substrate.

5.2.2 Focused ion beam process

The FEI Nanolab nova 200 and SMI-2050 FIB systems have been employed to pattern Bi nanostructures using Ga^+ ion beam milling and in-situ contact electrodes patterning. In the fabrication of Bi nanowires, FIB is a versatile tool that not only acted as a lithography tool, but also provides real-time SEM results.

More importantly, FIB was ideal for making bismuth nanowire devices due to its ability to remove bismuth oxide by successive scans of ion beams[121][118].

In the milling process of Bismuth films, an ion beam current of 10-50 pA and gun voltage of 30KeV has been considered to give the finest milling results[76]. To overcome the charging effect on the insulating substrate during the milling process, conductive layer coating, or charge neutraliser* can be used. By using SiO_2 substrates with 16 Au contact pads, the charging during I-beam and E-beam was found to be acceptable, suitable for fabricating structures as small as 30nm scale. The milling rate and milling depth of Bi in FIB can be verified with either tilted SEM view or by cutting a cross section profile in the FIB for analysis.

5.2.3 In-situ deposition of Pt contacts

The contact electrodes were deposited in FIB in high vacuum as bismuth can be readily oxidised in-air at room temperature[113]. In the FIB system, platinum electrodes can be aligned and deposited using electron beam induced deposition technique for making ohmic contacts to sub 100nm thick Bi nanowires.

*Electron flood gun that reduces charging on insulating substrates.

5.3 FIB experiments

During the development of the Bi nanowire fabrication process, experiments have been carried out in FIB machine to analyse, to understand, and to benchmark the capability of these FIB systems. These include the deposition of conductors and ion-beam milling of insulating, conducting and semi-metallic materials.

5.3.1 Conductor deposition

In a dualbeam FIB system, materials can be deposited onto the substrate by means of electron beam and ion beam induced deposition. Platinum and tungsten are the two types of conductors that can be deposited from the FEI nanolab nova-200 and SMI-3050 FIB machines at NCKU, Taiwan. During the deposition process, by irradiating the precursor gas with ion beam or electron beam, the non-volatile component of precursor remains on the surface as the deposited material.

The precursor gases used for Pt and W deposition were methylcyclopentadienyl platinum ($(CH_3)_3(CH_3C_5H_4)Pt$) and tungsten carbonyl ($W(CO_6)$)[76].

Conductors were normally deposited in FIB to form contact electrodes to semiconductor and nanowire devices. They can also be used as sacrificial layers during the ion beam process such as TEM sample preparation. In the dualbeam FIB system, electron beam deposition is normally preferred for conductor deposition due to the excessive material damage caused by the ion beam irradiation.

To understand the potential of electron beam deposition in FIB, a series of platinum deposition resolution tests have been carried out. Tungsten coated quartz and SiO_2 were used as substrates for these purposes. For single pixel nanowire deposition, linewidths of platinum nanowires can be controlled by the overlap setting and deposition thickness in the FIB software (As shown in Figure 5.6). It was found to be much easier to just adjust the deposition thickness setting as dose scales for FEI-200 system. In the deposition of single pixel line platinum nanowires, 5KeV electron beam acceleration voltage and 98pA of current was used. A nominal dose of $8mC/cm^2$ and magnification of 25,000X

has been determined experimentally as the optimal writing parameters for the smallest platinum structures.

From Figure 5.6, the smallest dimension platinum nanowires obtained with single pixel line using electron beam induced deposition was 25nm. It was achieved at an overlap factor of -100% (i.e. beam blanked for one pixel between two adjacent ones). The tilted view of this resolution test has also revealed that the nanowire was continuous when patterned with the above setting. Therefore, by adjusting the overlap percentage during the deposition of platinum nanowire, a line width reduction of up to 50% can be expected. Figure 5.5 shows the SEM image of the FIB E-beam deposited Pt nanowires in close up, where a gap of 11 nm between two adjacent structures was demonstrated. The E-beam induced deposition in a FIB system was found to have a very high yield, and can be used to deposit a wide range of materials with good substrate adhesion.

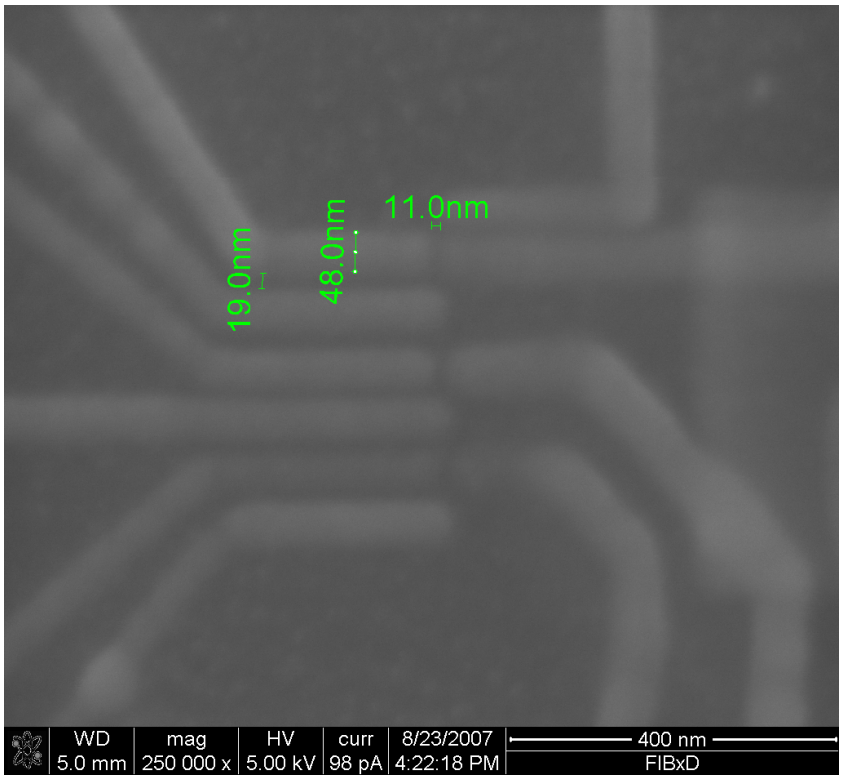
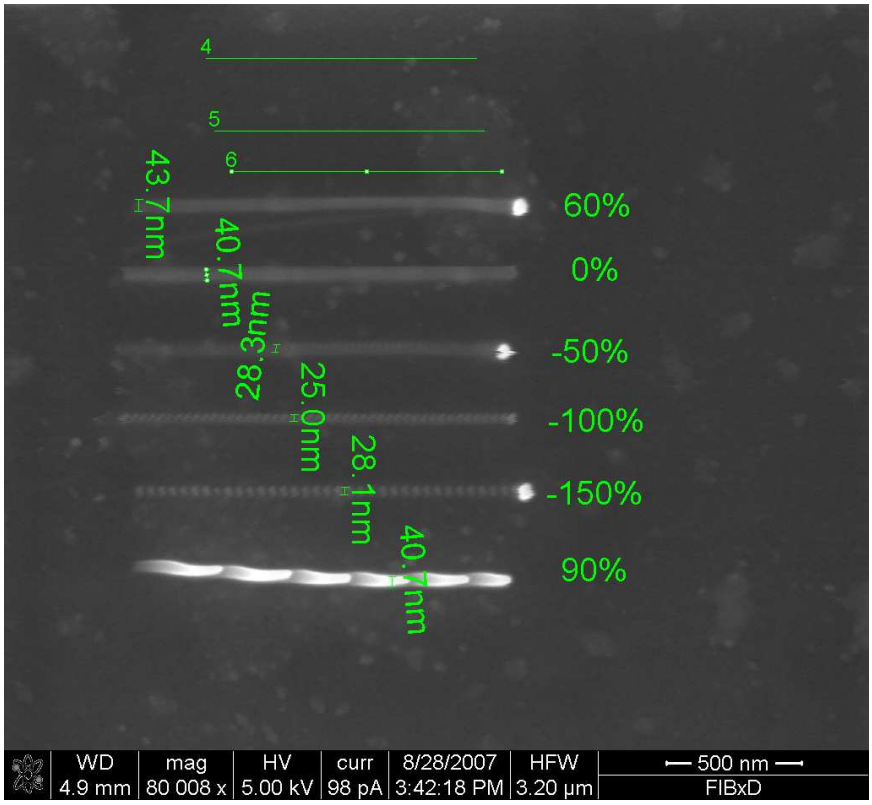
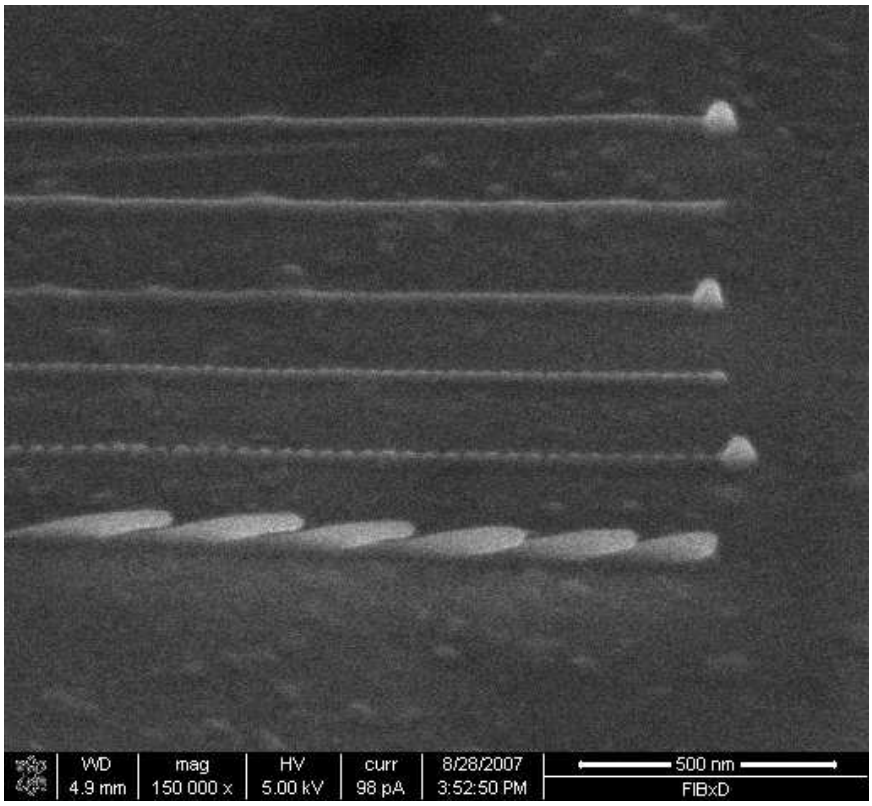


Figure 5.5: SEM image of E-beam induced Pt deposition of nanowires structures in close proximity, where Pt nanowires 48nm wide can be made with gaps as small as 11nm to nearby structures.



(a) Plane view.



(b) 52 degree tilted view.

Figure 5.6: SEM images taken from the 90° and 52° view showing electron beam induced Pt nanowire depositions. The linewidth of deposited nanowire (from 43.7nm to 25nm) can be controlled using overlap factor (60% to -100%).

5.3.2 FIB Milling

During the milling process, Ga^+ ions are accelerated at 5-30KeV and focused onto the surface of the sample by electrostatic lenses [76]. By configuring the ion beam current and dosage, the atoms of the surface material will be sputtered away rapidly. Because of the destructive nature of ion beam irradiation, the surface material of the sample suffers from a certain degree of Ga^+ ion implantation, and beam damage that might lead to surface amorphisation effects. In order to explore the potential of device making in FIB, a series of milling experiments were carried out including milling resolution tests (as shown in Figure 5.7), insulator milling, semi-metal milling and conductor milling. The resolution test pattern was created in Microsoft paint using bitmap format, containing single pixel lines in close proximity and nano and micro structures in arbitrary shapes. In this work, semiconductor milling experiments were not performed due to the limited number of FIB hours available and because of the well established databases that covers the FIB process of common semiconductors.

5.3.2.1 Insulator Milling

One of the advantage of using FIB machines for device making is the ability to deposit and mill insulators, such as SiO_2. For insulators like quartz and Si_3N_4, severe charging effect during the milling and deposition was observed. There are generally two ways of surface charge reduction methods in FIB system. These are dedicated charge neutralisers and e-beam scanning during the ion-beam milling process. However, charge neutralisers were not installed in both of the FEI and SMI FIB during the course of this work. The second method, on the other hand, was not suitable for E-beam deposition and nanoscale milling process.

To be able to perform milling into quartz, a thin conducive layer was pre-deposited onto the quartz substrate. Tungsten and PEDOT (Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)) can both serve as conductive layers that eliminate the charging effect on quartz during ion-beam milling. Although DC sputtered tungsten coated quartz shows no charging effect during the en-

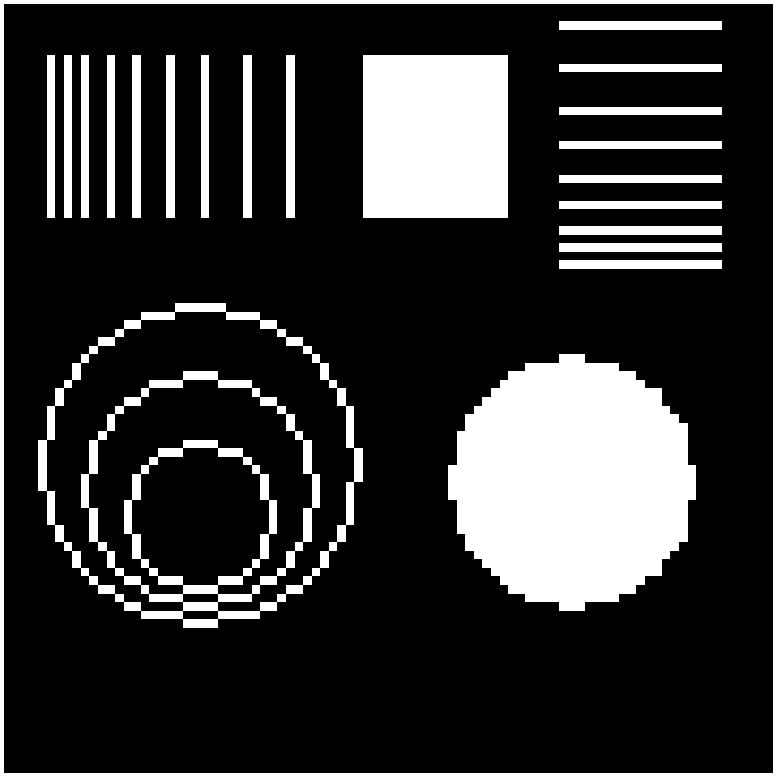
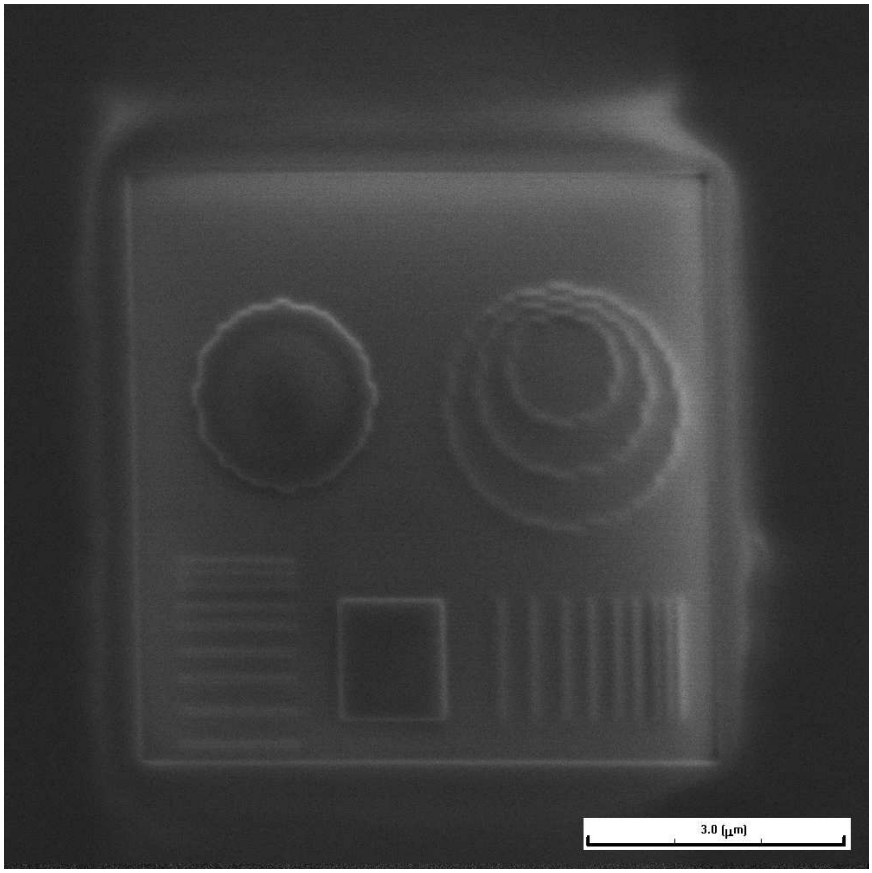


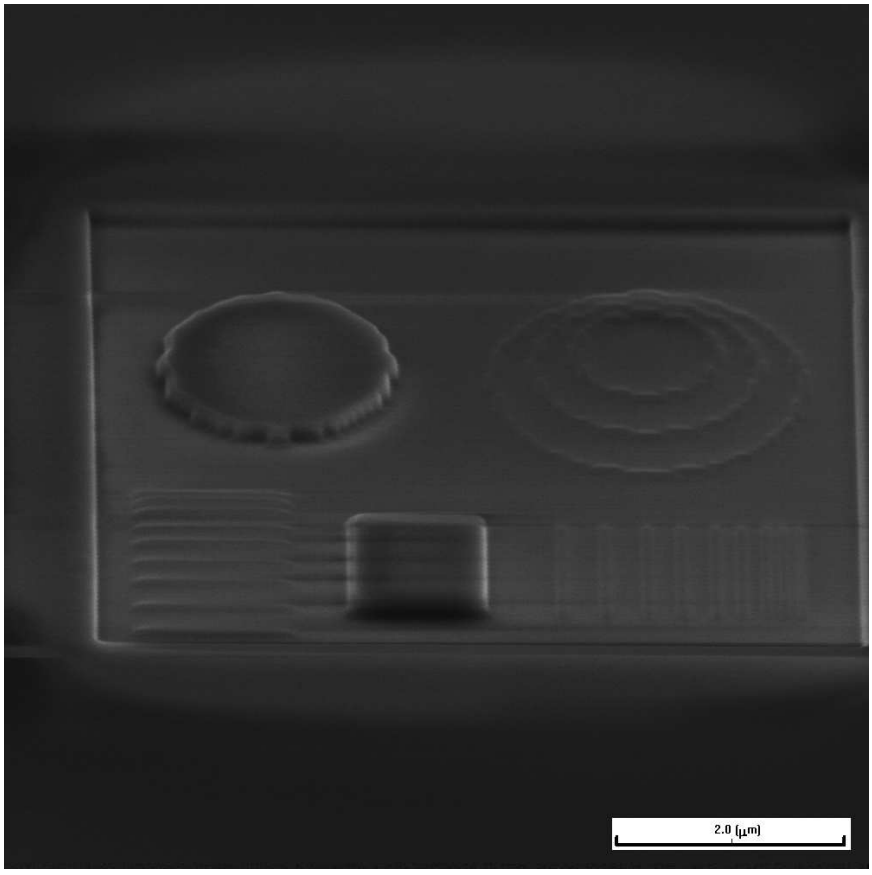
Figure 5.7: Bitmap FIB resolution pattern containing a total number of 10000 black and white pixels (100 by 100 pixels).

tire milling process, reactive ion etching or chemical etching will be required to remove the unwanted tungsten layer. In contrast, PEDOT is a hydrophobic conductive polymer that offers similar charge elimination effects with a relatively simple preparation and removal process. For the preparation of PEDOT coated quarts sample, it was spun onto quartz sample at 5000rpm for 1 minute. The film thickness was around 30nm after baking at 90°C on hot plate for 30 seconds. In our experiment, the sacrificial PEDOT layer can be readily removed in 40°C DI water held for 30 seconds after the FIB process.

Figure 5.8 shows the FIB milling results of quartz with 30nm of PEDOT coating, where the milling depth was 100nm. Similar experiments were repeated on plain quartz without any conductive coating and no successful nanowire structures were formed due to severe charging effects.



(a) Top view.



(b) 52 degree tilted view.

Figure 5.8: SEM images of quartz milling resolution test, with PEDOT anti-charging layers showing lines and circular with dimensions between 50nm to 2μm.

5.3.2.2 Bismuth milling

In this experiment, bismuth film was thermally evaporated through an EBL opened PMMA window on SiO_2 substrate with sixteen predefined gold contact pad structures. Figure 5.9 shows an example of a SEM image of bismuth film in the middle of sixteen gold contact pads, where the overlap region between bismuth film and contact pads were utilised to compare the I-V results with and without the mill-and-fill process, a process developed for making ohmic contact to Bi nanowires. The bismuth films were thermally evaporated onto SiO_2 substrate at a rate of $1\mathring{A}/s$, vacuum level of 10^{-5}Torr and current setting of 81A. From the AFM image (shown in Figure 5.4), the deposited polycrystalline bismuth film has grain sizes in the 70-120nm range.

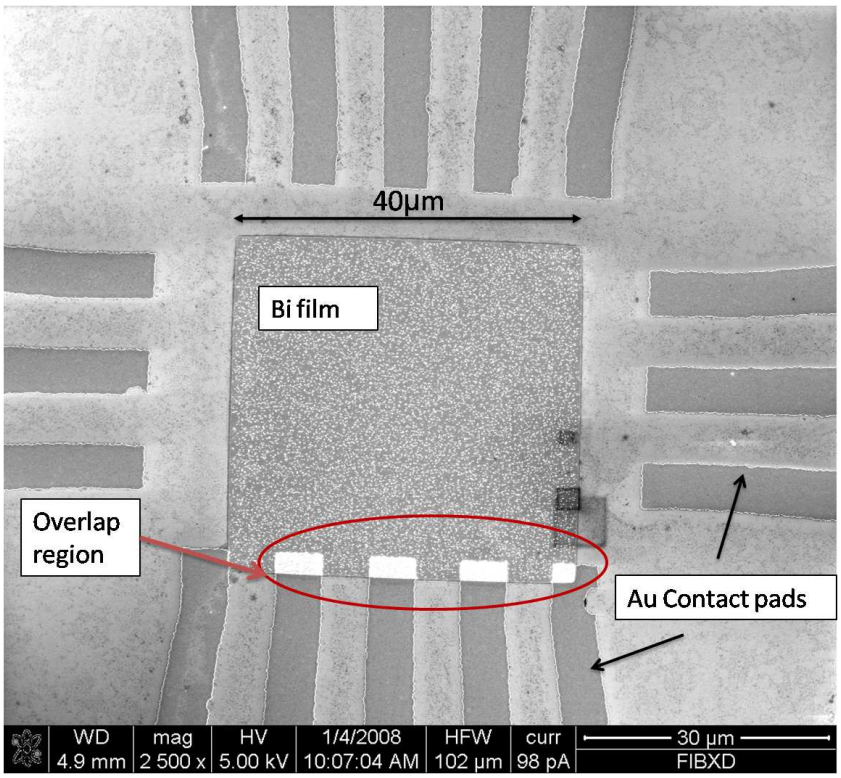


Figure 5.9: SEM image showing thermally evaporated bismuth film on a SiO_2 substrate with pre-defined Au contact pads.

In the milling of Bi films, several experiments have been performed to optimise the milling parameters including the dose, dwell time, overlap and beam current. Petit[122] has demonstrated the use of FIB to fabricate Bi nano Hall sensors with wire widths in the 50nm regime. The Bi structures were milled with

30KeV Ga ion beam at 20nA, and 1ms dwell time. Similar parameters have been tested in both the FEI nanolab nova-200 and SMI 3050 system and it has been found that by using a smaller current of 10-50pA, Bi nanowires as small as 20nm were observed. Figure 5.10 shows the SEM image of a resolution test of bismuth milling in SMI-3050 system. The Bi nanowires structures formed by single pixel milling method were successfully fabricated. The milling depth achieved was 40nm using the following conditions: ion beam voltage of 30KeV, dwell time of 100μs, and i-beam current of 50pA. To further demonstrate the resolution of bismuth milling for various structures, the logo of the University of Canterbury (UOC) has also been milled on Bi coated Si substrate. The SEM images of UOC logo are shown in Figure 5.11, where the smallest line-width obtained is around 10nm (the character "U" in Figure 5.11(b).

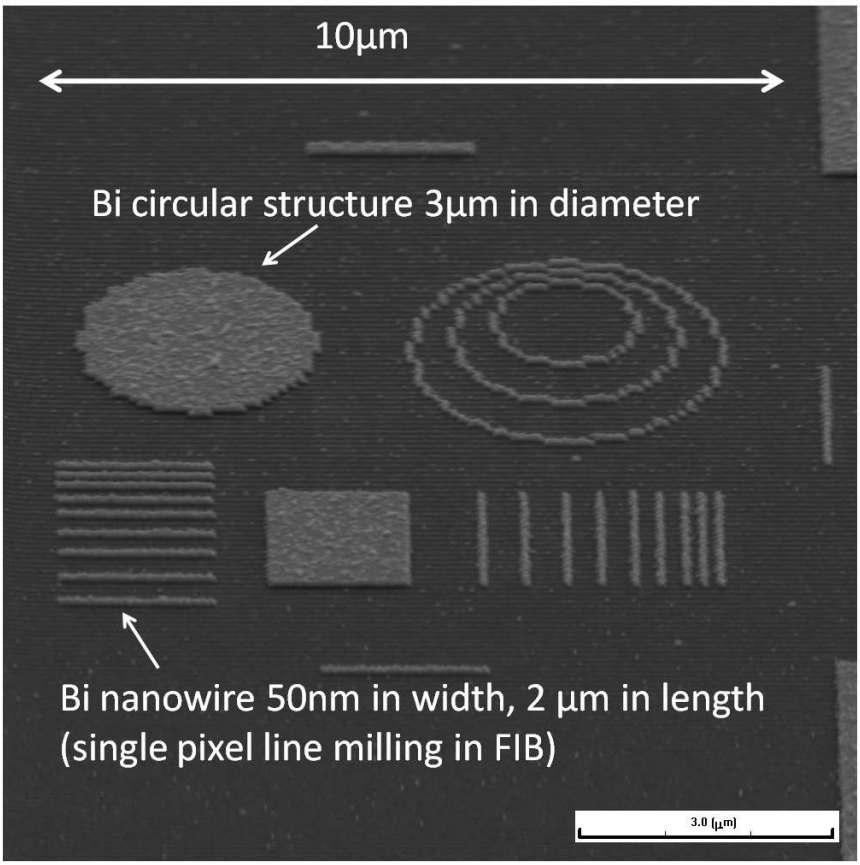
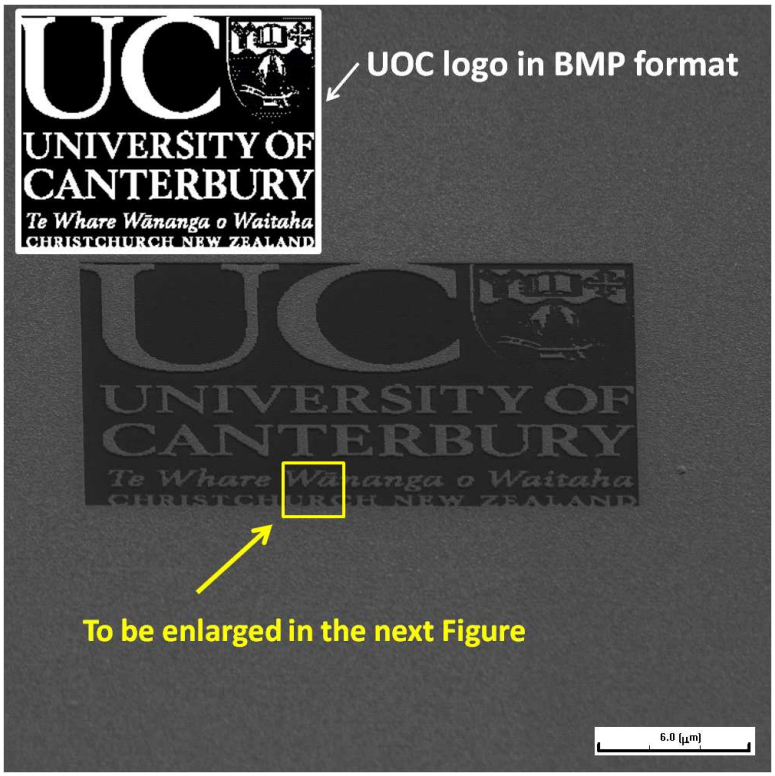
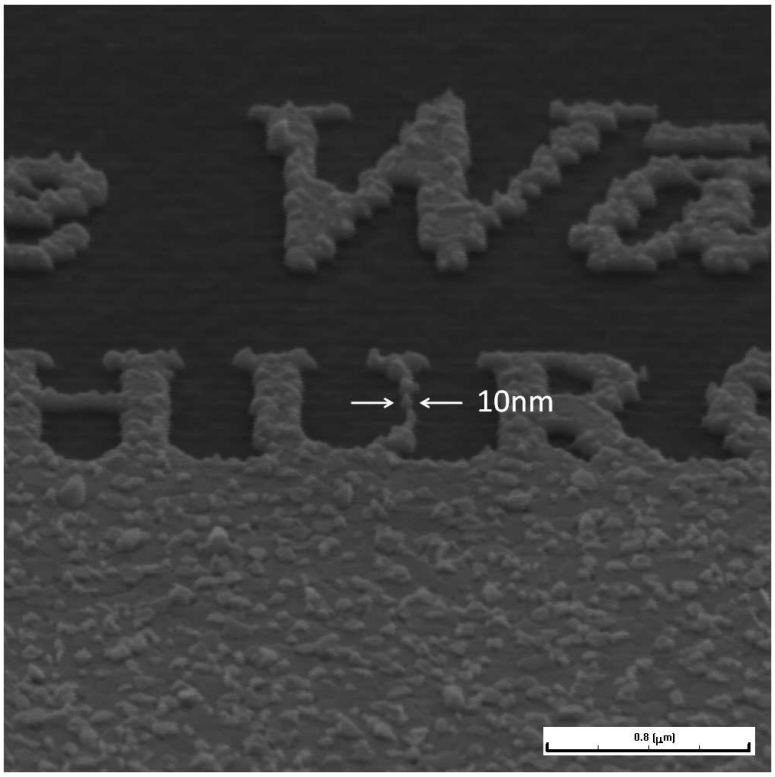


Figure 5.10: SEM image showing resolution test pattern of Bi milling on SiO_2 substrate using SMI-3050 FIB system. Bi nanostructures with dimensions ranging from 50nm to 3μm can be milled using 30KeV Ga^+ ion beam with beam current of 50pA.



(a) SEM image of Bi UOC logo on Si substrate. Insert shows the University of Canterbury (UOC) logo in Bitmap format, and yellow box represents the area containing 10nm features on the next image.



(b) Closeup view of milled structure showing 10nm features

Figure 5.11: SEM images showing FIB milled bismuth structures representing UOC logo on Bi coated Si substrate.

5.4 Bi device fabrication

Bismuth has drawn great attention in many fields including thermalelectronics, Hall effect sensing, and transistor applications due to its unique properties. Among these many research activities, only few groups have used FIB milling to fabricate Bi based devices[122]. In this study, the fabrication process of Bi nanowire devices are presented. The fabrication steps can be summarised into Bi thin film deposition, Bi milling, contact deposition, mill-and-fill processes for ohmic contact purposes, as shown in Figure 5.12.

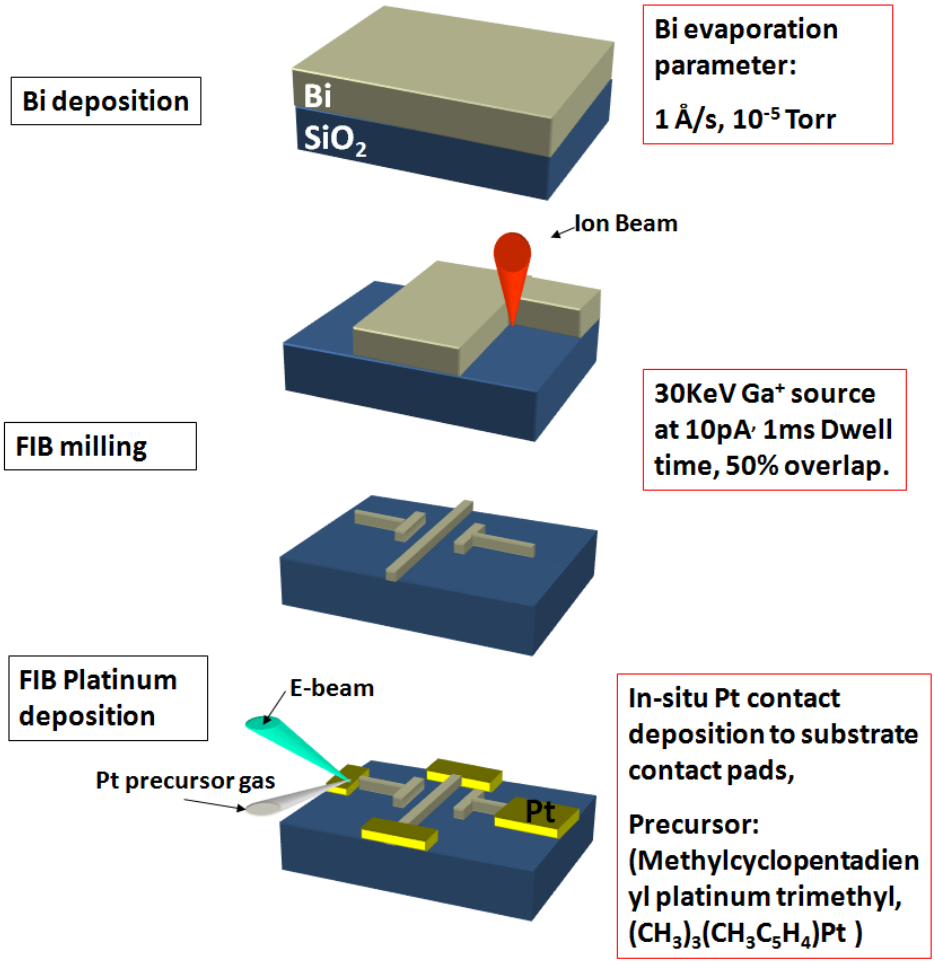


Figure 5.12: Fabrication process involved in the development of Bi nanowire structures.

5.4.1 Bismuth nanowire structures

In the bismuth nanowire milling, two FIB systems have been employed, where their optimised parameters for the highest resolution milling of bismuth can be

summarised in Table 5.1.

Table 5.1: Bi milling parameters in both FIB systems.

FIB parameters	SMI-3050	FEI-200
Write field	60μm	60μm
Nominal vol/dose (m^3/C)	1.6	0.643
I-beam	30KeV	30KeV
I-current	50pA	10pA
Dwell time	1ms	10μs

Sub 50nm wide Bi nanowires have been successfully fabricated using both of these machines. Figure 5.13 shows the SEM image of a 40nm Bi nanowire fabricated using SMI-3050 system. During the FIB process, the nanowire width can be controlled by varying the dosage, the overlap factor, the number of pixels that represent nanowire width in the bitmap (BMP) pattern, or by adjusting the ion-beam current and beam dwell time. Figure 5.14 shows the SEM image of a 50nm Bi nanowire based transistor like structure fabricated using SMI-3050. The two lateral gates were designed to produce a localised electric field that governs the flow of current through the 50nm channel.

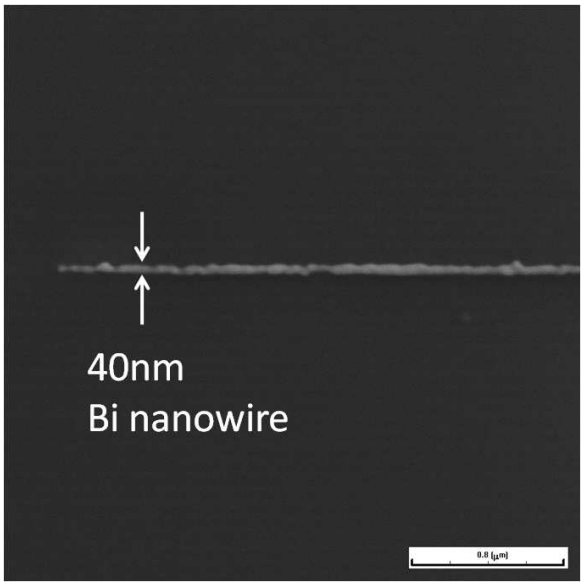


Figure 5.13: 40nm Bismuth nanowire milled using SMI3050 FIB system.

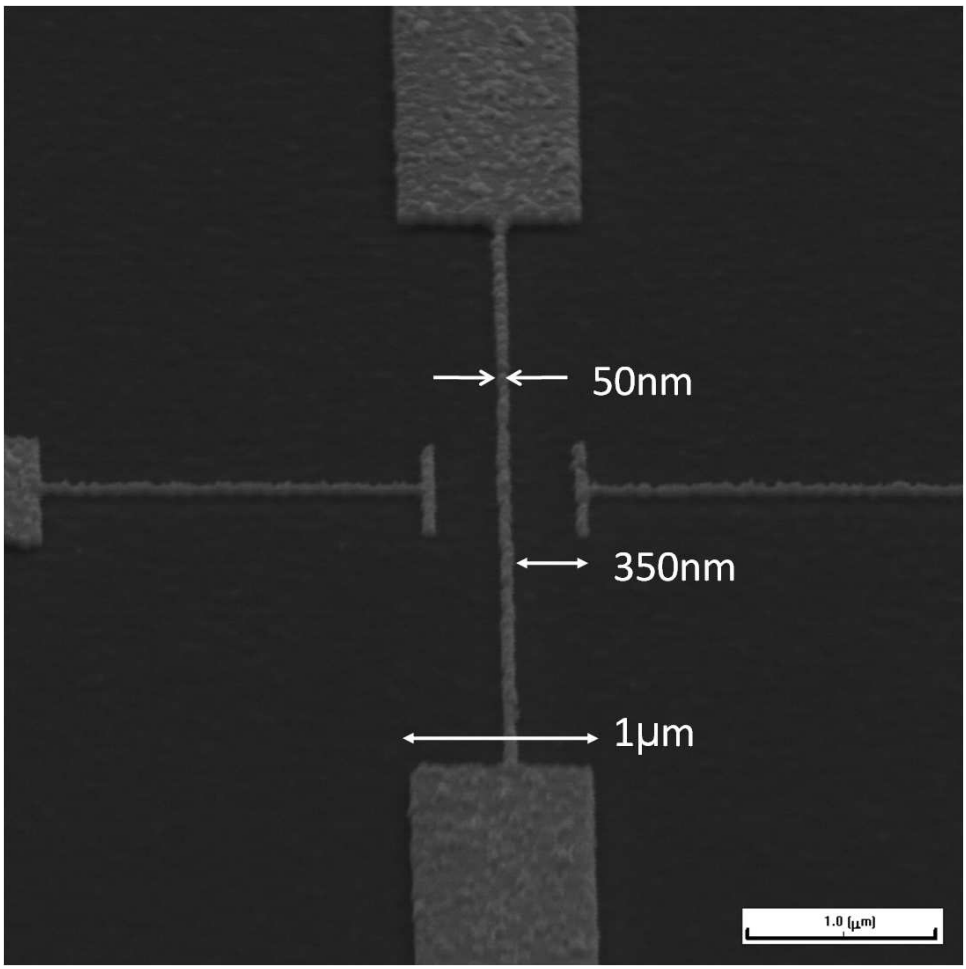


Figure 5.14: 50nm Bi nanowire transistor structure fabricated using FEI FIB system.

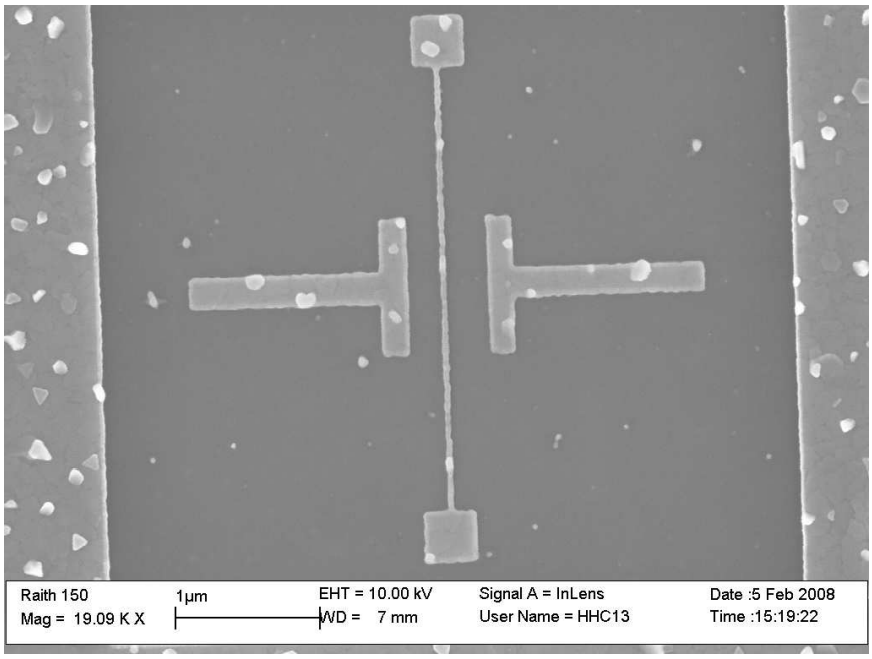
After applying Bi milling parameters as shown in Table 5.1, a Bi nanowire transistor structure with its smallest dimensions in the 30nm scale has been fabricated. Figure 5.15 shows the SEM images of this device, where the 5μm by 5μm nanowire structures were milled with a dosage of 2.572 m^3/C at 10pA, 30KeV Ga^+ ion beam and 10μs dwell time. In the SMI-3050 system, a dwell time of 1 ms would result in smallest nanowire features for milling bismuth. Whereas for the FEI system, by changing the dwell time setting from 10μs to 1ms, the nanowire width has increased from 30.55nm to 42.38nm.

5.4.2 Ohmic contact fabrication

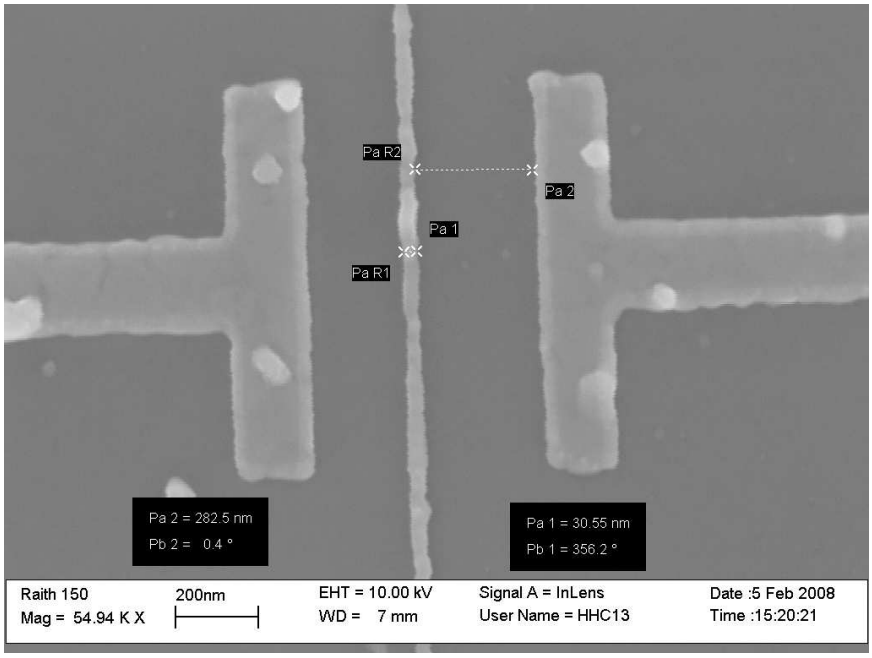
One of the challenging factors involved in the fabrication of bismuth devices is to form ohmic contacts. Bismuth is known to have a native oxide layer up to 10nm thick, resulting in high contact resistances[119]. Cronin[118] has pioneered a number of methods for Bi oxide removal processes including chemical etching, high-temperature gas-phase reduction method and focused ion beam scanning process. Among these processes, focused ion beam scanning is the most effective method as it allows in-situ deposition of contact electrodes after the oxide removal process. For other techniques, the oxide layer can usually grow back at room temperature in air in a few seconds. As a result, FIB systems have been utilised extensively from the milling of Bi structure to the creation of ohmic contacts using by electron beam induced metal deposition.

5.4.2.1 Contact electrode deposition

Based on the result of E-beam deposition experiments, Pt nanowires ranging in widths from 200nm to 400nm, and 10μm to 40μm long have been deposited in FIB in-situ to connect the Bi nanowire structures to the pre-defined Au contact pads for device probing. Figure 5.16 shows a SEM image of Pt contact deposition experiment on SiO_2 substrate, where the 400nm wide and 200nm thick Pt nanowire was deposited onto Bi nanowire using E-beam deposition at 5KeV, 98pA at 20,000X magnification.



(a) SEM image taken at 19,090X magnification.



(b) SEM image taken at 54,940X magnification.

Figure 5.15: Bismuth nanowire structure with a width of 30.55nm, and two lateral gates located 285nm from the nanowire fabricated in FEI-200 system.

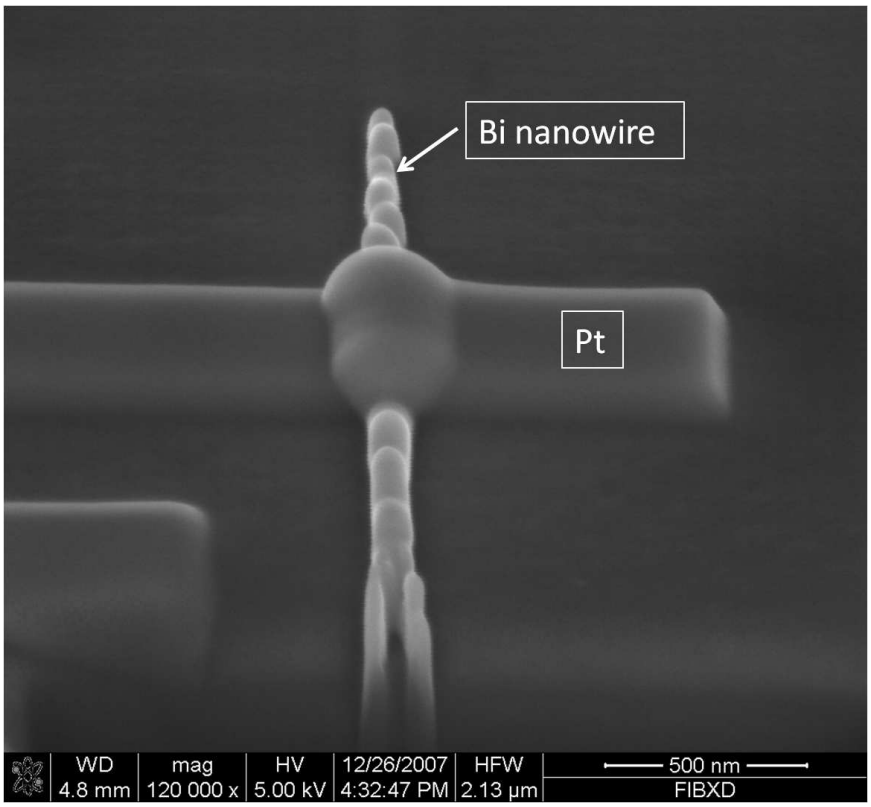


Figure 5.16: SEM image taken at 52° showing in-situ Pt contact deposition on Bi nanowire using FIB. The thickness and width of deposited Pt were 80nm and 200nm respectively.

5.4.2.2 FIB oxide removal process

Cronin[118] demonstrated the removal of Bi oxide that has grown on a 200nm thick Bi nanowire using successive scans of Ga ion beam, as shown in Figure 5.17. From it we can see that by employing Ga^+ beam irradiation, the surface oxide of nanowire 200nm in width was removed after 5 scans. Similar attempts have been carried out using the FEI nanolab nova-200 FIB system. However, due to the smaller dimensions (sub 50nm) of our Bi nanowires, both of the cores and the oxide of nanowires would be sputtered away in a few scans of ion beam.

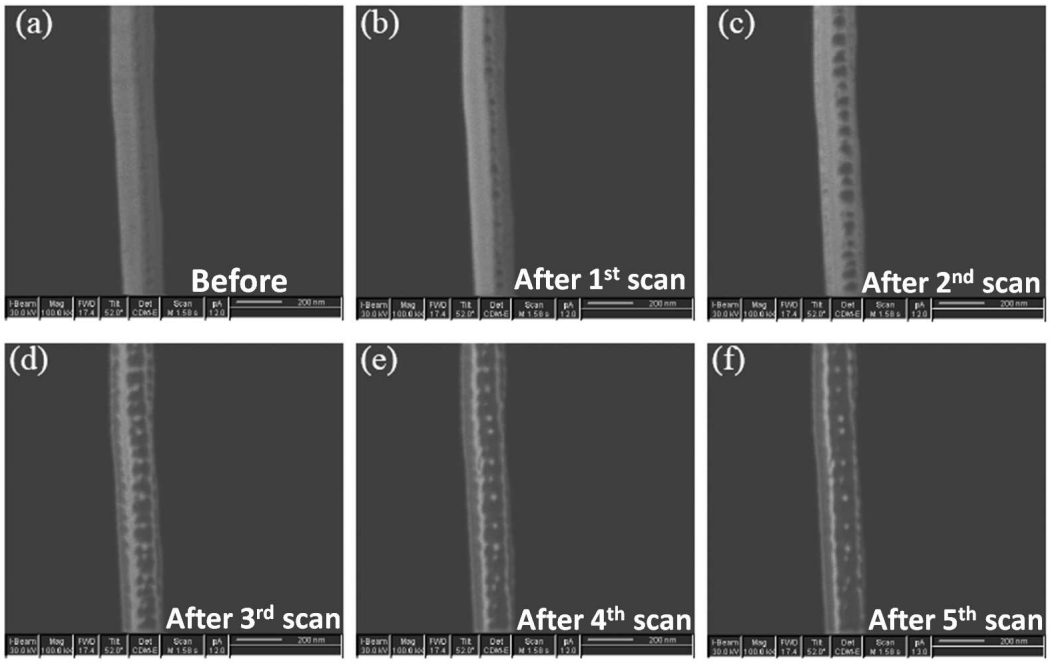


Figure 5.17: Oxide removal process of a 200nm Bi nanowire using successive scans of ion beam, adopted from[11].(a) shows the nanowire prior to ion beam scanning, and (b) to (f) shows the image after ion beam scanning from two times up to 5 times.

5.4.2.3 Mill and Fill process

From previous research work, the oxide removal process using FIB scanning was not viable for nanowires smaller than 100nm in diameter. A more complicated process in FIB has to be developed to form ohmic contact to sub 100nm Bi nanowires. In this process, Pt contacts were first deposited on top of the Bi nanowire region. A small hole was then ion-beam milled on the contact region

followed by filling the hole with Pt deposition[118]. Numerous experiments have been spent on developing this technique to optimise the parameters for this process. It requires very high accuracy of alignment between the electron and ion beam, minimum beam drifting between two deposition processes, and optimised etch rate for the Pt and Bi material. An FIB based process has been developed in the current work to form ohmic contacts to 30nm-50nm bismuth nanowires. The optimal parameters for both FIB systems are shown in Table 5.2

Figure 5.19 shows the SEM images of the mill-and-fill experiment carried out on the SMI-3050 FIB system. In this experiment, a tungsten layer was first deposited onto bismuth film using electron beam induced deposition in FIB, followed by the milling of nano hole into the Bi film layer and E-beam deposition of second tungsten layer that filled the nano-hole. We called this technique the mill-and-fill process as it described the cutting and filling of metal layers that form intimate contact to the Bi structures. From Figure 5.19(c), it is clear to see that the nano-hole on the first tungsten layer has been successfully milled into the bismuth layer, and the second layer of tungsten has made good contact to the bismuth layer through the milled nano-hole. From Figure 5.19(c), we can see that the surface of the exposed bismuth region though the nano-hole has been partially sputtered, resulting in removal of the surface oxide of bismuth to form a good contact to the second tungsten layer.

Similar experiments have also been performed using the FEI nanolab nova-200 system, where Pt contacts were deposited onto Bismuth nanowire in-situ. Figure 5.18 shows the SEM images of the in-situ mill-and-fill process carried out in FEI nanolab nova-200, where the nano-hole has been milled into the bismuth nanowire region. The contact between Bi nanowire and Pt electrodes were found to be ohmic, the two point resistance measurement will be discussed in Chapter 6.

Table 5.2: Mill-and-Fill ohmic contact process

FIB system	SMI-3050	FEI-200
For contact deposition:		
Contact material	W	Pt
Write field	60μm	60μm
E-beam	1KeV	5KeV
E-current	9500pA	98pA
Dose factor	5X	6X
Target thickness	100nm	100nm
For milling:		
Write field	60μm	60μm
I-beam	30KeV	30KeV
I-current	50pA	10pA
Dose factor	8X	2X
Milling depth	120nm	120nm
Dwell time	200μs	10μs
For filling:		
Contact material	W	Pt
Write field	60μm	20μm
E-beam	1KeV	5KeV
E-current	9500pA	98pA
Dose factor	5X	6X
Target thickness	100nm	100nm

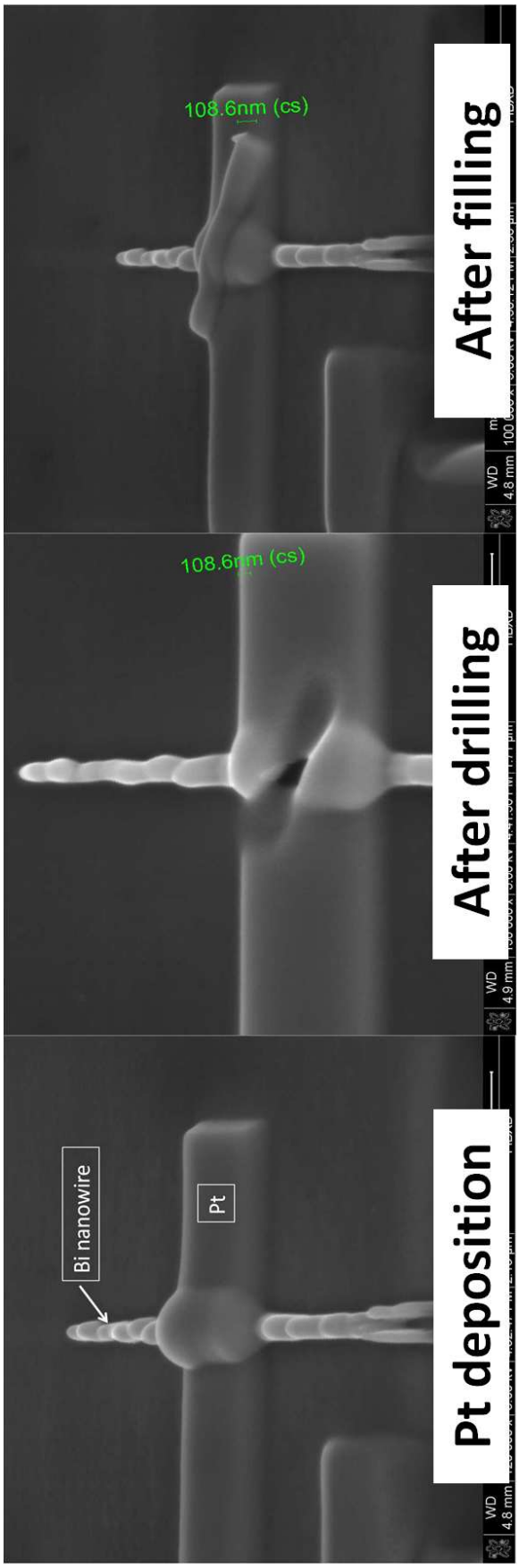
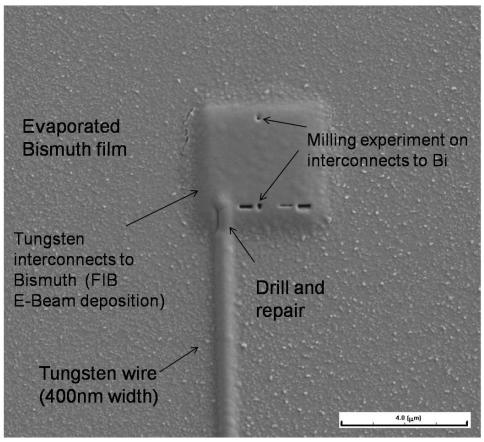
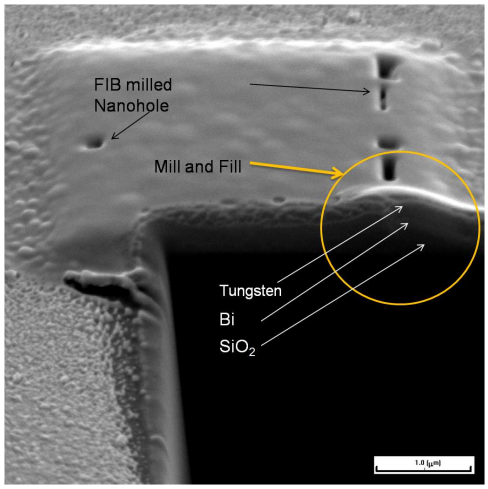


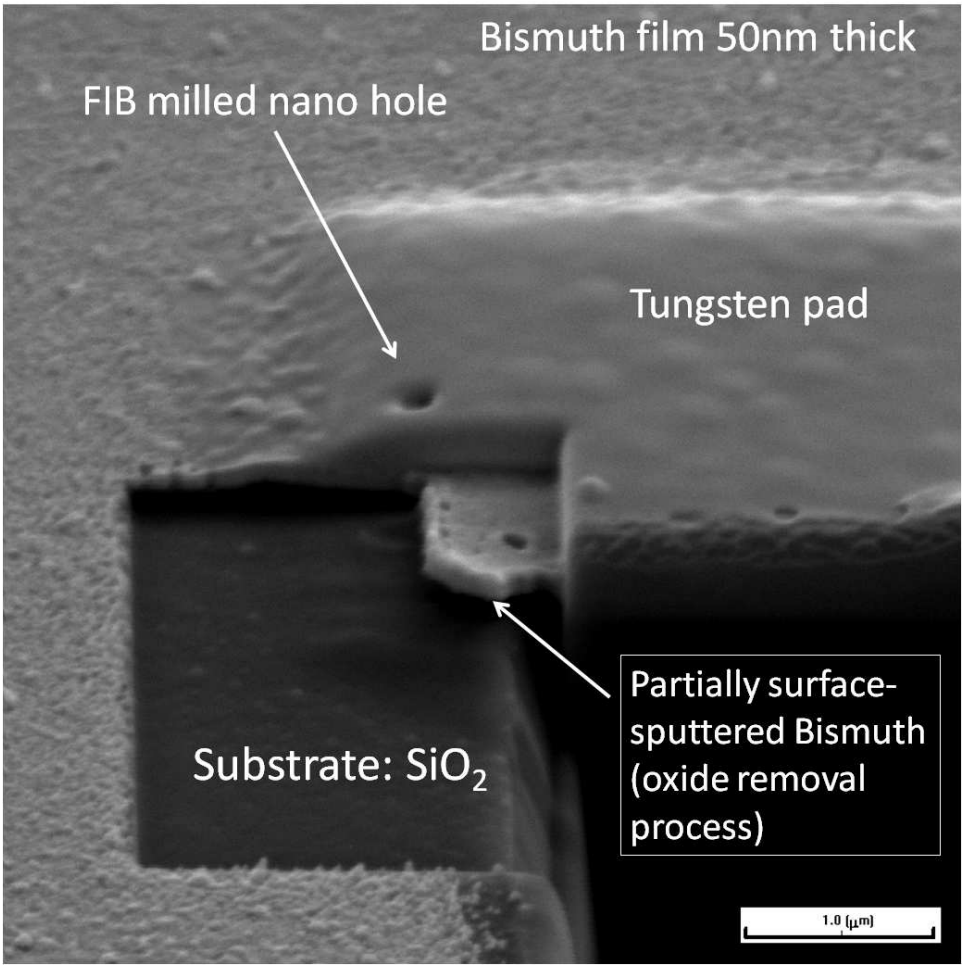
Figure 5.18: Ohmic contact to Bi nanowires using mill and fill process(FEI-200). The pt wires were deposited using E-beam deposition in FIB system.



(a) SEM image showing multiple layers deposited and milled in a Mill-and-fill experiment.



(b) Cross section view 1



(c) Cross section view 2

Figure 5.19: Mill-and-Fill experiment performed on Bi coated SiO_2 substrate using SMI-3050. These SEM images show different layers deposited and milled to form good ohmic contact to the underlying Bi film on a SiO_2 substrate.

5.5 Direct platinum dot array depositions

During my work on Bi device fabrication, I took the opportunity to explore the use of FIB in making nano dot structures with electron beam induced deposition. By employing our experience in EBL and FIB of single pixel lines induced dot exposures, we have successfully demonstrated the capability of fabricating nanoscale dot array structures in an ultra high density fashion.

Two dimensional nanoscale dot arrays have the potential for applications in the field of optoelectronic devices, biochemical platforms, and magnetic storage medias. In fact, the development of magnetic storage media based on nano dot array structures have demonstrated ultra high data density greater than $1Tb/in^2$ using bit patterned media[125]. This has opened a new avenue for the next generation data storage devices.

EBL has previously been employed for pattern nano dots in close proximity for bit patterned medias, where dot structures with 12.5nm diameter, 25nm pitch can be obtained[126]. However, the functionality of these devices depend closely on the dot arrangements, physical dimensions and reproducibility. Although one can apply nanoimprint technology for high volume fabrication of these dot structures, the nanodot structures in the prototype mold, have to be highly ordered and homogenous. Unlike EBL, the fabrication of nanodot array structures in FIB does not depend on resists, and the development process. By using the right precursor, ferric materials can be deposited in a high resolution and efficient manner using electron beam induced deposition in FIB systems.

During the research of bismuth nanostructures, the deposition of Pt wires was found to undergo interesting pixel-to-dot magnification effects, suitable for large scale metal dot array fabrications. We have demonstrated an efficient technique for fabricating nanoscale dot-arrays based on this phenomenon. Moreover, the high precision stage of FEI nova nanolab 200 FIB system allowed us, for the first time, to form complicated structures by stacking stack multiple layers of fabricated nanodot arrays.

5.5.1 Pixel-to-dot pattern magnification

In this experiment, Pt deposition was carried out using an electron beam at 5KeV, 98pA, and dose of 12.5mC/cm^3 with 60μm write field size. The smallest unit of Pt nanoscale dots can be deposited in FIB by means of fixing the beam at one single spot at a time, forming Pt dots structure based on the time and the dose. This can also be achieved by exposing a single pixel nanowire structure with the variation of pixel step sizes (as shown in Figure 5.6). However, in the FEI nova nanolab 200 FIB system, an alternative approach to fabricate nano dot arrays was to adjust the magnification of bitmap patterns[†].

By importing a 2-bit (black and white) bitmap image containing known number of pixels, each pixel will be registered as a single dot structure prior to electron beam deposition. More interestingly, we have found that the pitch and diameters of nanodots can be controlled by means of bitmap magnification factor and dose respectively. Figure 5.20 depicts the pixel to dot pattern magnification process. By importing a 5 by 5 pixels black square bitmap image into the FEI-200 pattern generator, and by enlarging this 25 pixels structure into a 500nm by 500nm square, the resulted deposition can yield nano dot arrays containing 25 nano dots with 100nm pitch.

The bitmap test patterns were created in rectangle structure containing 440 pixels (11$\times$40 pixels). Initially, this pattern was enlarged in FEI-200 pattern generator to 1μm by 4μm prior to E-beam irradiation, where the write field and deposition thickness was set to 60μm and 100nm respectively. Figure 5.21 shows a Pt dot array fabricated using pixel-to-dot deposition in FEI-200 with E-beam dose of 12.5mC/cm^3. These highly ordered periodic dot structures were 50nm in diameter, 82.5nm pitch and 80nm in height, representing a data density of 100Gb/in^2.

Next, we have demonstrated the scaling effect of these dot arrays by adjusting the magnification of the same bitmap pattern. By scaling the bitmap into 2μ by 8μm, a dot array with 100nm diameter, 185nm pitch has been successfully

[†]This technique was found only applicable with the FEI FIB system, in SMI3050 FIB system a result of enlarge the bitmap image will be deposition over the whole area instead of separating them into fine dots.

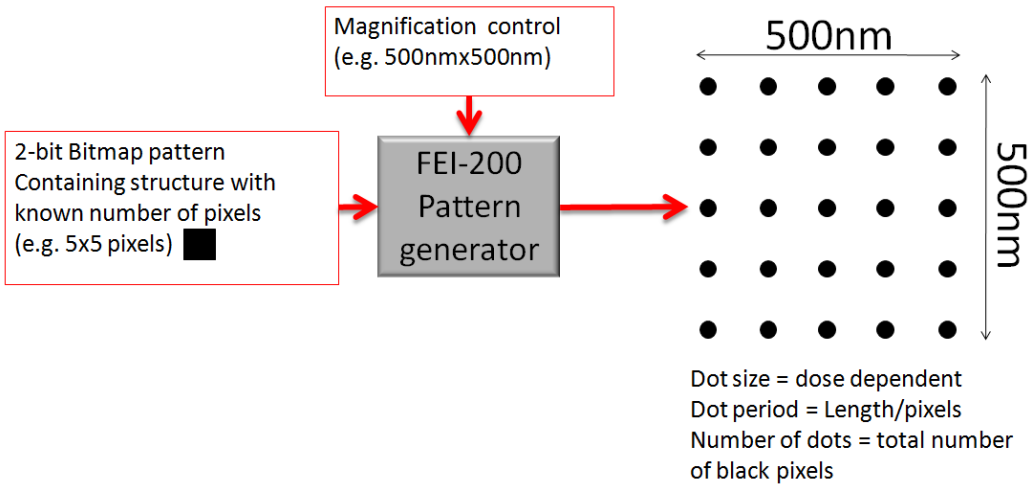


Figure 5.20: Pixel-to-dot pattern transfer technique employed in the fabrication of Pt nanoscale dot arrays.

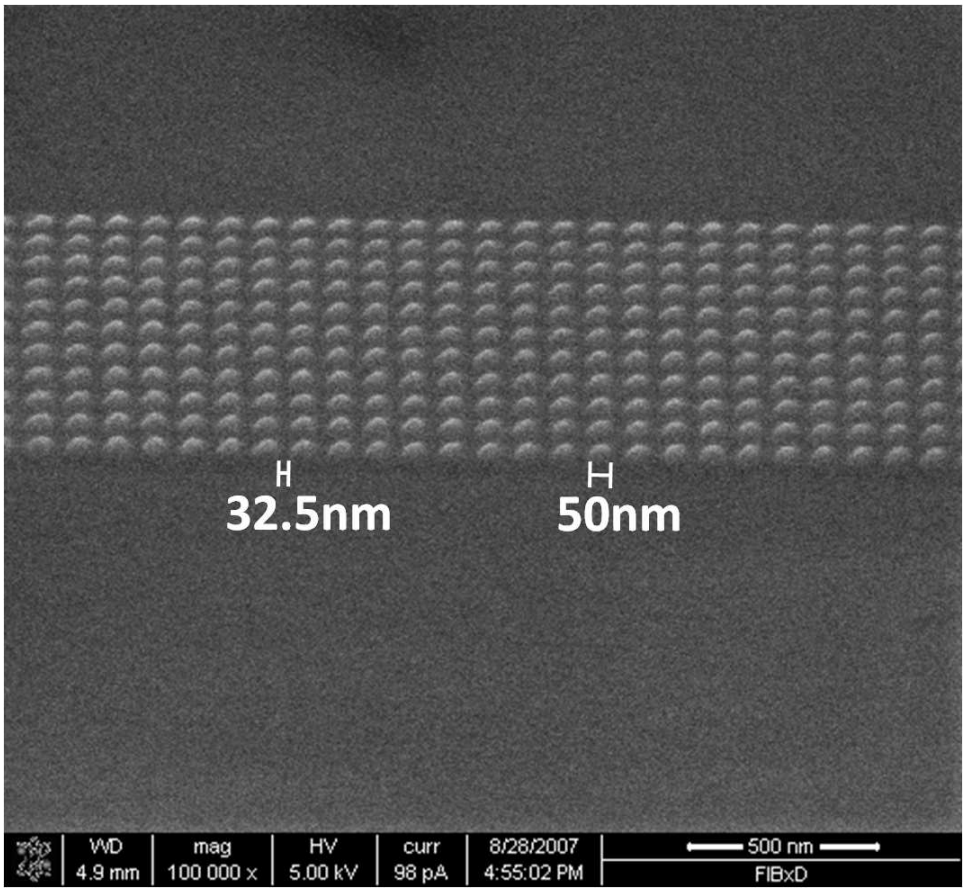


Figure 5.21: SEM image taken at 100,000X showing E-beam deposited Pt nano dot array of 50nm dots, 82.5nm pitch on Si substrate.

deposited, as shown in Figure 5.22. The fabricated dots were found to have exact shapes and the process can be repeated with relatively high yields. In terms of large scale patterning, FEI-200 system can address up to 1M pixels. This is equivalent to a maximum dot array size of 100μm by 100μm, containing 1M dots 50nm in diameter, 100nm period.

For large area patterning of dot structures, this technique can be employed to reduce the number of registered pixels included in the bitmap pattern for conventional dot array patterns by a factor of two, as blank pixels were not required to address for dot spacing in pixel-to-dot magnification process.

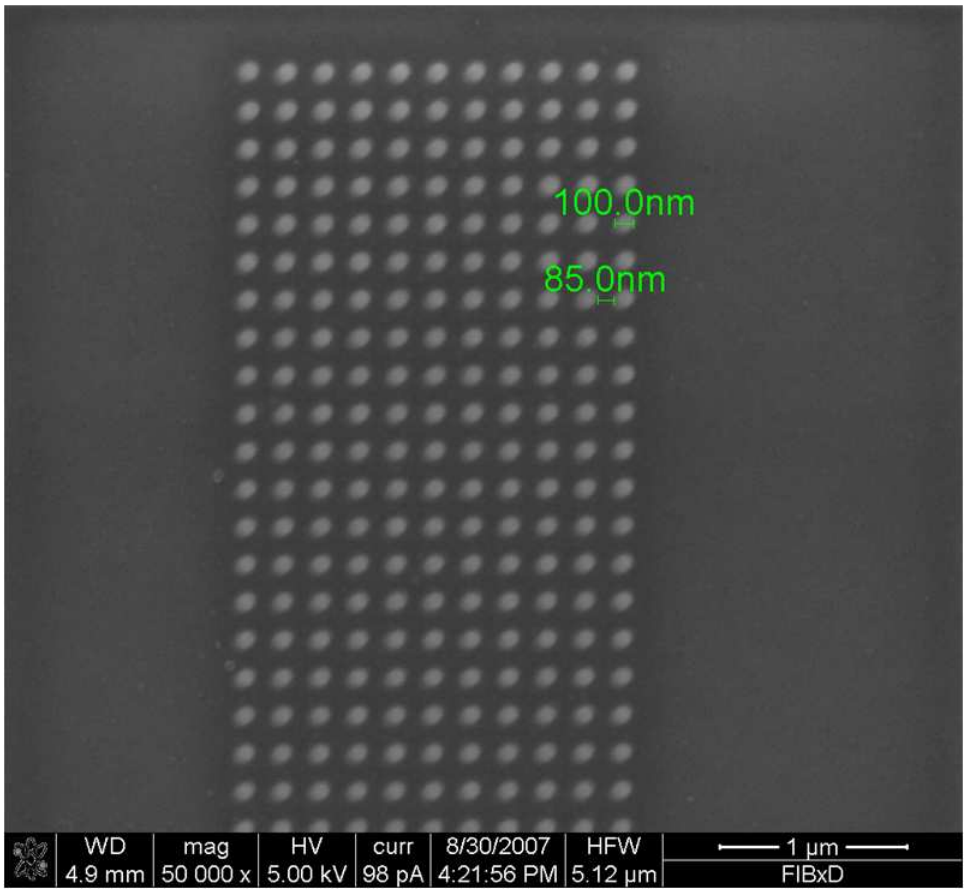


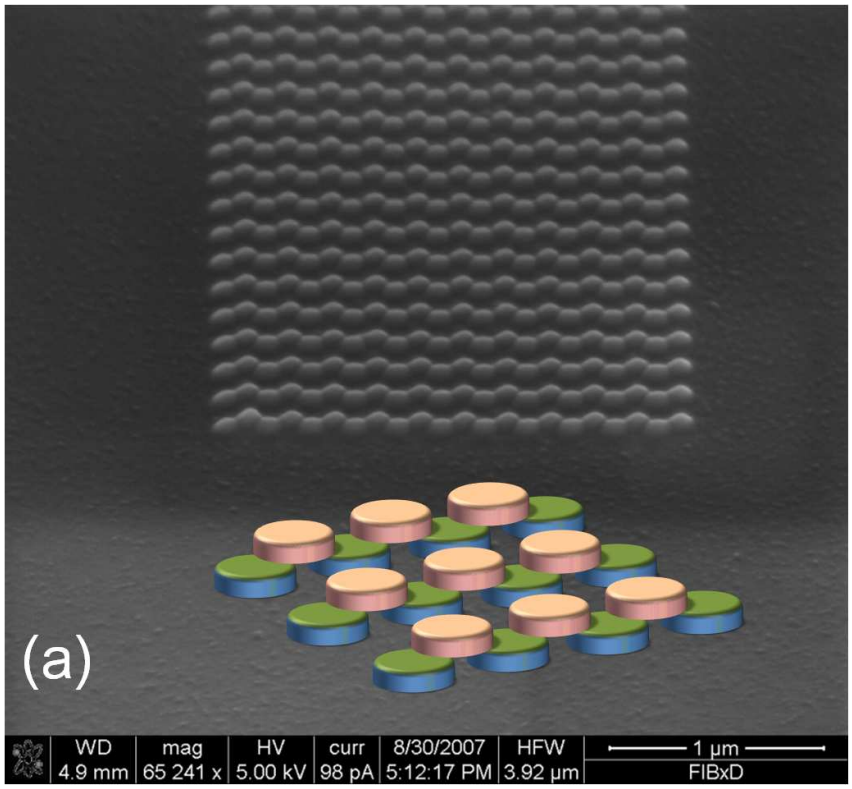
Figure 5.22: SEM images showing E-beam deposited Pt nano dot array of 100nm diameter dots, 185nm pitch on Si substrate. This was achieved by scaling a bitmap pattern of 11$\times$40 pixels into a 2μm by 8μm using FEI-200 pattern generator.

5.5.2 Dot array stacking

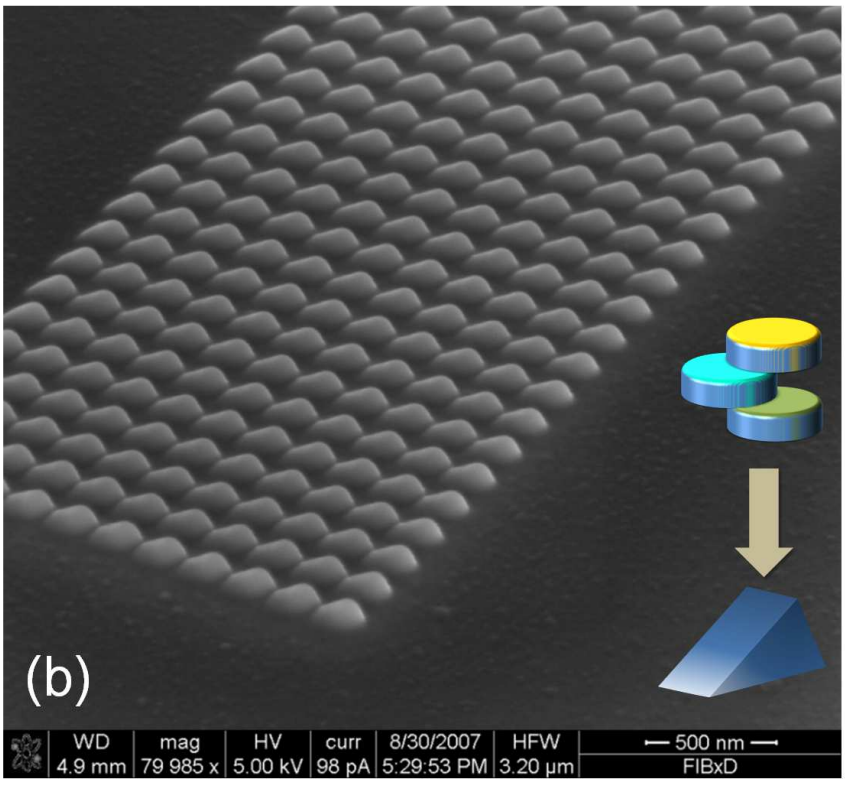
In this study, dot arrays stacking based on direct depositions of metals using pixel-to-dot technique have also been explored. The high resolution high accuracy alignment of FEI-200 FIB has allowed the stacking of multiple layers of dots to be performed, resulting in a highly ordered 3D structures. Figure 5.23 shows the multilayer dot array stacking result of two layers and three layer respectively. These structures were stacked based on dots of 100nm in diameter, 185nm pitch, deposited on 10nm tungsten coated Si substrate using electron beam at 5KeV, 98pA, with dose of 28mC/cm^3 and deposition thickness of 100nm. Interestingly, the three layer stacking of dot arrays (Figure 5.23(b)) formed a 30° tapered structure instead of a three layer dot stacking structure. This is mainly due to the overlay of the three stacked layers. Further optimisations are possible to perform three-layer stacking of dot arrays with a controlled slope.

5.6 Summary and discussion

Although bismuth has been widely researched during the last decade, challenging factors such as establishing high quality nanowire growth technique and forming good ohmic contacts to electrodes have made Bi based devices difficult to fabricate and synthesis. Without reliable fabrication techniques, meaningful properties of these devices are not possible. The invention of FIB has opened a convenient way not only to mill nanoscale bismuth nanowires but also to form good ohmic contacts to them. In this project, 30nm wide bismuth nanowire has been successfully fabricated using FIB milling technique. In order to form good ohmic contact to these nanoscale Bi nanowires, a mill-and-fill method has been developed. In terms of Bi thin film deposition, similar surface morphology containing Bi grains ranging from 100nm to 200nm in dimensions were observed on SiO_2 as reported by Ramadan[123]. Kumari[124] has indicated an increase in grain size with reduced deposition rate using thermal evaporation. As an effort to improve the film quality, a deposition rate as low as $1\mathring{A}$/s was used and we were not able to reduce it any further due to the low melting temperature (271°C).



(a) Two layer stacking of nano dot arrays.



(b) Three layer stacking of nano dots, resulting in highly ordered 3D structures with 30° tapered shape

Figure 5.23: SEM images showing multilayer dot arrays stacking based on 100nm diameter dots of 185nm pitch

In the development of optimised milling parameters for 50nm Bi nanowires, an ion beam current as low as 10pA was employed. Along with the use of single pixel line milling, this low current has enabled us to form 10nm wide Bi nanowires, smaller than the reported value (20nm) reported from Petit[116] using 1pA. The processes involved in the fabrication of 30nm wide Bi nanowires were reliable and repeatable, and the yield for delivering a continuous nanowire using FIB was found to be much better than that of EBL based fabrications.

The real challenge of this experiment lies in the fabrication of ohmic contacts of sub 50nm Bi nanowires. The ohmic contacting in FIB requires ultra high alignment accuracy between the deposition of contacts and precise control over the milling depth during the mill-and-fill process. In addition, for each sample, the dose required for high quality Pt deposition and the milling depth used for mill-and-fill process have to be determined individually. These issues have resulted in time consuming processes for developing samples that yield correct electrical properties. In Cronin's work[118], undesired Pt deposition halo[‡] effects were observed during the ion beam induced Pt deposition process. By employing a dual beam FIB system, we were able to deposit Pt using electron beam induced deposition where no halo effects were observed due to the narrow spread of fine electron beam at 5KeV. We have also explored the ability to directly deposit nanoscale dot arrays using E-beam induced deposition. This has provided an alternative solution for patterning ferric magnetic storage medias with ultra high density. We have demonstrated the potential of employing pixel to dot techniques for larger area pattern, where a density of $100Gb/in^2$ was obtained. Experiments have been performed to determine the resolution limit of nanodot array deposition on Quartz samples. Without the charge dissipation layer, the minimum dot array features fabricated were 30nm diameter, 50nm pitch, representing a data density of $250Gb/in^2$.

[‡]The electrodes shorting effect due to the wide spread of ion beam in an ion beam induced deposition process.

Chapter 6

Characterisation results

Previous chapters have presented the fabrication techniques and experiments for the development of metallic and semi-metallic nanowire structures for resistance and gate effect measurements. The characterisation of these devices will allow us to investigate the electrical properties and any switching behaviour for different types of nanowire structures and materials.

In this chapter, the characterisation of two transistor structures are studied, the silver stripe and the metal nanowire transistors. First covered are the I-V measurement of Ag nano stripe devices, designed to offer sub 10nm thick silver stripe for gate effect measurements. Due to the very low yield fabrication involved in the deposition of dielectric coating between the stripe and gate electrodes, only IV characterisations were performed. Next covered is the electrical characterisation of nanowire based transistor devices. These wires (made from Ag, NiCr, and Bi with Au contacts) are made by the EBL and FIB based processes with their widths ranging from 15nm to 1μm.

In order achieve high sensitivity and high accuracy IV measurements, dedicated semiconductor analysers with aluminium shielded probe stations were employed. The electrical properties of these metal stripe and nanowire structures revealed higher resistances than their bulk resistance values mainly due to the grain boundaries scattering and surface scattering[127][128]. Main challenges occurred during these measurements were the voltage offset during the four point measurement and the low signal to noise ratio (SNR) for low resistance metal wires.

In terms of gate effect measurements, Ag and NiCr nanowires with widths in the range of 15nm to 30nm have been tested. As expected, no influences on the conduction were observed when gate voltages ranging from -5V to 5V were applied. This is because the widths of the fabricated nanowires are still large compared to the screening length of the metals. We have also for the first time investigate the gate effect of Bi nanowire (225nm diameter) fabricated using FIB systems. As expected, transistor like switching effects were not observed as these dimensions are much greater than the screening length of Bi (40nm).

This chapter details the measurement setups, the I-V results from two point and four point analysis, and the gate effect measurement results of thin film and nanowire structures made from Ag, NiCr, and Bi.

6.1 Electrical measurement setup

Electrical properties of fabricated metallic structures were measured using HP4155A semiconductor parameter analyser by means of two point, four point resistance and transmission line measurements. These metallic nanostructures were fabricated with arrangements suitable for various device probing using semiconductor analysers and micro-manipulaters. The contact resistance can be determined directly based on transmission line measurement (TLM) using the setup illustrated in Figure 3.12(a).

Nanowire and nano stripe structures were found extremely fragile for passing current, especially for sub 20nm diameter nanowires. Experimental results indicated the yield for all four contacts to be working simultaneously was relatively low. As a result, small current (a few hundred pA) was used to determine the resistances in aluminium shielded boxes to reduce the electromagnetic, photoelectric, and acoustic noises.

The HP4155 semiconductor analyser is equipped with four source/monitor units (SMU)[129], capable of monitoring current while acting as a voltage source, or monitoring voltage while sourcing current, and as a common node, monitoring current when used as ground. A probe station was employed for direct contact to the gold bonding pads without the need for wire bonding processes*. The same setup can be used to carry out the transmission line measurements by taking the resistance values over a set up contacts with known nanowire lengths. Table 6.1 summarises the resolutions for HP4155A for the most sensitive measurements, where the voltage and current must be lower than 2.2V and 10nA respectively[129].

In this work, all the measurements were carried out in either single or double sweep mode with long integration (>320ms/step)[129]. Figure 6.1 shows the common setup for two point resistance measurement employed for electrical characterisation. In the setup, SMU1 was configured as either voltage source or current source, whereas the other probe, SMU2 was configured as common

*For Y-branch transistor characterisation, either 1 or 2 external probes were required to modulate the gate voltage from Keithley source meter through wire bonded pads.

Table 6.1: Resolutions for SMU output and measurement in HP4155A.

Mode	Resolution
Voltage source (VS)	100μV
Voltage monitor (VM)	2μV
Current source (CS)	100fA
Current monitor (CM)	10fA

mode (ground) for current measurement (I_F).

The setup for a more accurate resistance measurement, the four point resistance measurement, can be found in Figure 6.2. In this setup, four SMUs were employed, allowing the resistance of the nanowire to be measured independently to contact resistances. In order to monitor the voltage drop across the nanowire region, two SMUs (SMU2 and SMU3) were configured as fixed current sources with a current of 0 , while SMU1 and SMU4 were set as a current source (for sourcing I_F) and ground. Figure 6.3 shows the setup for gate effect measurements of thin metallic nanowire structures. The experiment was carried out by monitoring the conductance variation due to the presence of external electrostatic fields supplied by the metallic gate structures. In the setup, SMU1, SMU2 and SMU3 were configured as constant current source (I_{DS}), ground, and voltage source. The gate leakage current were monitored throughout the period to identify any gate leakage resulted from high gate voltages. Similarly, for Y-branch transistor structure, the current diversion experiment has been setup as in Figure 6.4. In the setup, SMU1 and SMU2 were configured as voltage source for current measurements, SMU4 was employed as constant current source for drain-and-source current, I_{DS}, whereas the gate voltages were supplied by external Keithley 2400 source meters.

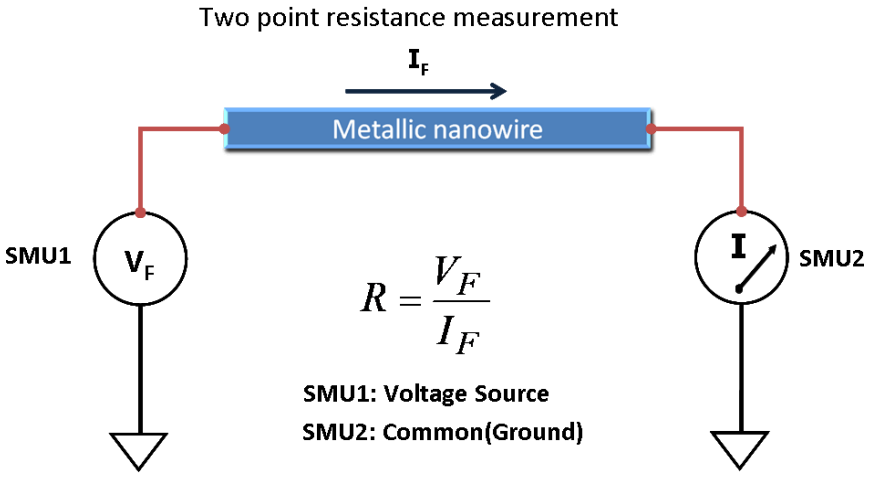


Figure 6.1: Setup showing the operation modes of SMUs for two point resistance measurement using HP4155A semiconductor analyser.

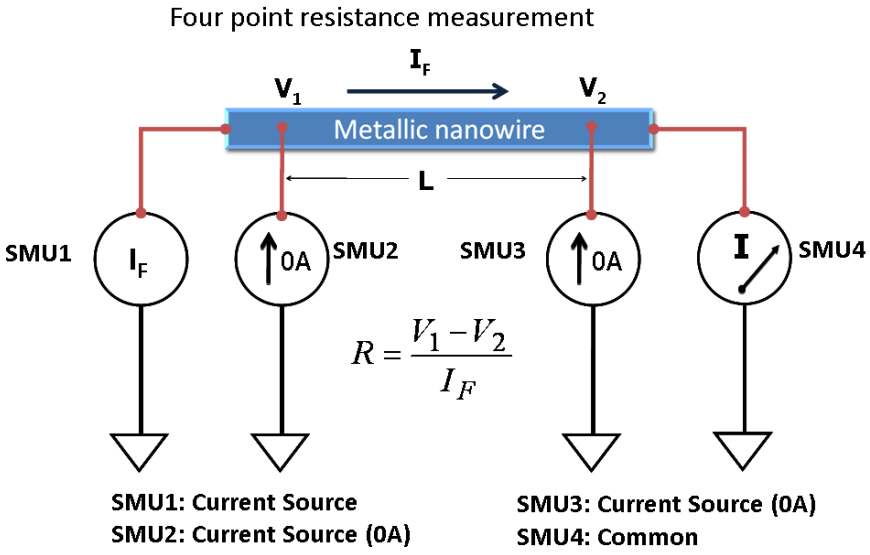


Figure 6.2: Setup showing the operation modes of SMUs for four point resistance measurement using HP4155A semiconductor analyser.

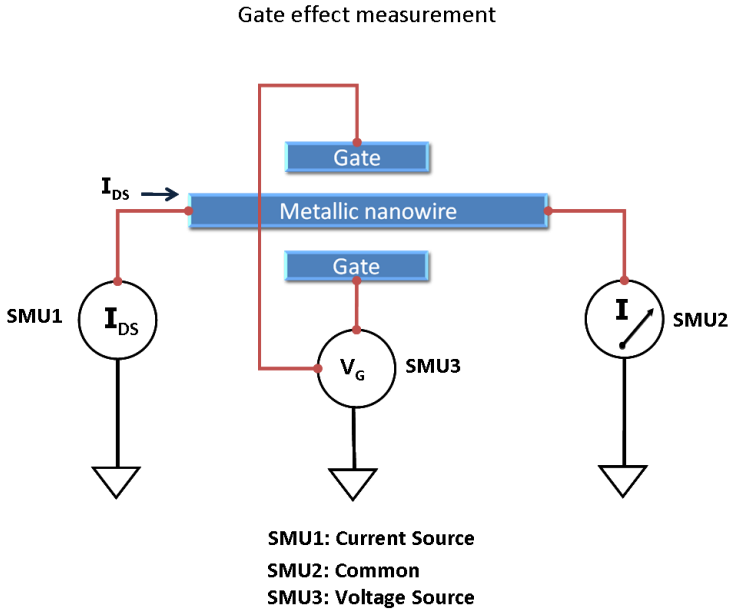


Figure 6.3: Setup showing the operation modes of SMUs for electric field effect measurement.

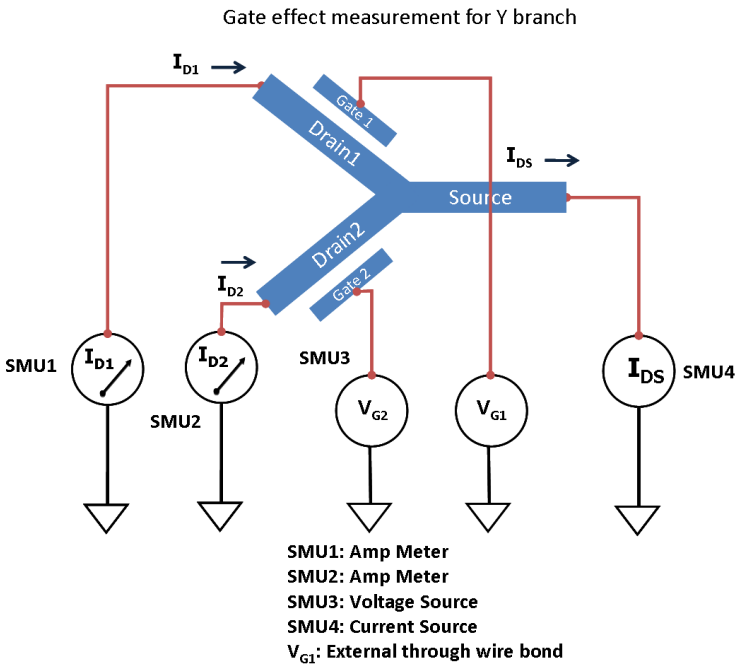


Figure 6.4: Setup showing the operation modes of SMUs for current diversion experiment based on the electric field effect of Y shaped nanowire structures.

6.2 I-V characteristics of Ag nano stripes

Section 4.5 illustrated the fabrication process of Ag thin film structures using Edwards Auto-500. This device was designed to explore the possibility of electric field penetration for ultra thin films, with thicknesses ranging from 7nm to 20nm, difficult to achieve using current EBL approaches. Although we were not able to perform gate effect measurements on this type of device due to the porosity of RF sputtered SiO_2 layer, we were able to study the I-V characteristics of very low resistance, high quality Ag film using numerous approaches. The thin Ag layer was RF sputtered onto Si_3N_4 and SiO_2 substrate using 50W of power and Ar in Edwards Auto-500 sputtering system. With a deposition rate of 1.2 $\mathring{A}$/s, the minimum thickness required for a conducting Ag film was experimentally determined to be 7nm.

To characterise the Ag nano stripe structures, Au contact electrodes and bonding pads were deposited using photolithography and thermal evaporation, followed by the subsequent lift-off process. The bonding regions were designed 200μm by 200μm in dimensions to allow direct manipulator probing using the HP4155A analyser. Figure 6.6(a) shows SEM image of one Ag thin film structure with electrodes connected for four point resistance measurement.

The contact resistances have contributed significantly to the total resistance of Ag thin film structure in a two point measurement setup. In order to evaluate the contact resistances, transmission line measurement (TLM) was performed using the setup in Figure 3.12. Figure 6.5 presented the result for TLM for 10nm Ag film in three different lengths. The contact resistance was determined to be 54Ω for each contact electrode. The sheet resistance (Ω_s) of these Ag nano-stripe devices can be determined from the slope of TLM graph, with a value of 0.58Ω/μm.

Figure 6.6(b) shows the two point I-V characteristics for 4μm wide, 10nm thick Ag film structures with resistance increased in proportion to their lengths. The resistance values in bracket are the predicted values based on their sheet resistance determined from Figure 6.5, calculated using $R = \Omega_s \times L + R_{contact}$. Where L is the length of the wire, Ω_s is the sheet resistance from the TLM mea-

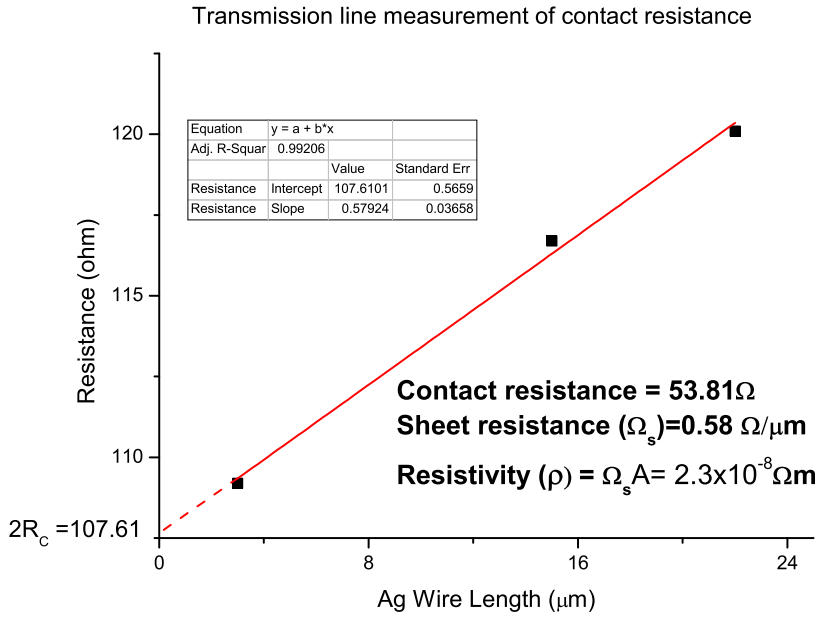


Figure 6.5: Transmission line measurement for contact resistance evaluation. The dashed line represent the predicted intercept used to approximate the contact resistance.

surement, and $R_{contact}$ is the contact resistance. In the two point I-V, the measured resistances agreed closely with the calculated one using the sheet resistance determined from the TLM method.

Figure 6.7 shows the four point I-V result for Ag wires 8μm long, 10nm thick for two different widths. The measured resistances (determined using the setup in Figure 6.2) were found roughly two times larger when compared to the calculated resistance using the formula $R = \rho \times L/A$, where ρ is the resistivity of Ag nano stripe from Figure 6.5, L is the length of stripe and A is the cross sectional area of the stripe. Although two point resistance measurement showed good match to the calculated value, four point measurement revealed increase in resistance, giving more accurate result to the true strip resistances.

The increases in resistances in a four point measurements were mainly due to the small dimension of film thickness. The electron mean free path of Ag (52nm) is almost five times larger than the film thickness, resulting in grain boundary scattering and surface scattering that led to an increased resistance[130]. These scattering effects were first studied by Fuchs and Sondheimer[127] in

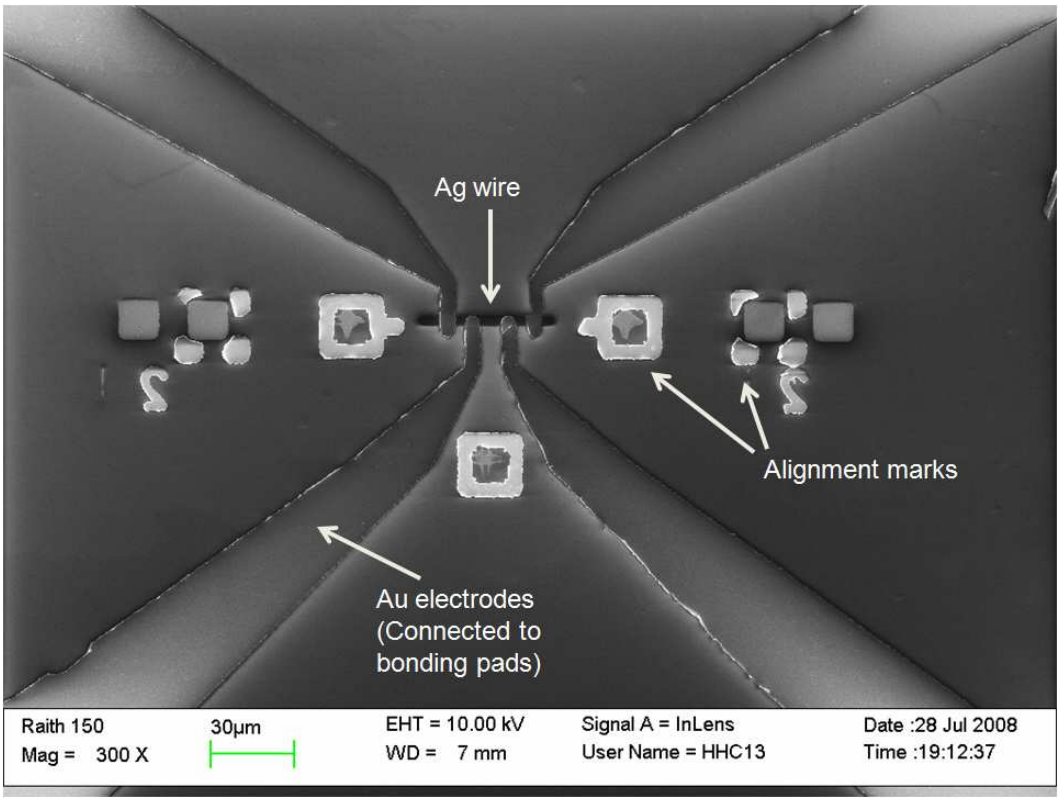
1952. Where they described the resistivity of a thin film by a surface scattering model for film thickness smaller or comparable to the electron mean free path (EMFP). Later, Mayadas and Shatkes[128] studied these effects and presented the effect of the scattering at grain boundaries on the conduction of electrons for thin films with thickness smaller than their EMFP.

6.3 I-V characteristics of metallic nanowires

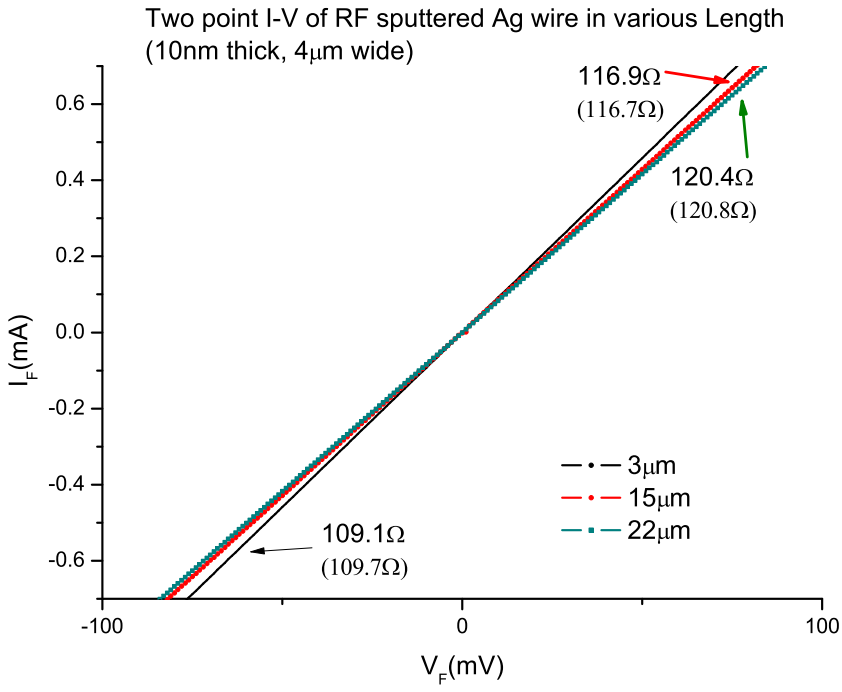
Throughout this study, nichrome ($Ni_{0.8}Cr_{0.2}$) and silver have been used extensively for benchmarking the EBL process for nanowire based transistor structures. Due to the smaller grain size of alloys like NiCr and AuPd, nanowires can be easily metallised by these materials using ultra thin trenches on EBL patterned PMMA, resulting in smaller linewidths over nanowire made from Ag and other transition metals. The adhesion of NiCr, in addition, was found to be much stronger than Ag, Al, or Au on SiO_2 and Si_3N_4 substrates[131]. This allowed for a high success rate in metal lift-off of NiCr, suitable for making nanowires as small as 12.5nm using Raith 150 EBL system. The high resistance of Nichrome nanowire has made it less favourable to be used for metallic transistor devices that require high transconductance channels. However, the yield of fabricating a continuous and conductive NiCr nanowire, was found much higher than Ag nanowire using the same fabrication processes.

Although nichrome is known for its high resistivity[132] when comparing it to transition metals, we have demonstrated the ultra high current density conduction for NiCr 15nm diameter nanowire with a dissipated power of 1.9mW (greater than 1×10^8 A/cm^2[†]). For these reasons we have studied the characteristics of those nanowire structures made from NiCr material. The NiCr nanowires were metallised using thermal evaporation at 10^{-6}Torr with a deposition rate of up to $3\mathring{A}$/s. Figure 6.8(a) shows an example of the two point I-V characteristics, where the calculated resistances using bulk resistivity value (ρ=1.5$\times 10^{-6}\Omega$m [134]) were shown in brackets. The measured resistances are

[†]For single wall nanotube, current density can be as high as 1×10^9 A/cm^2[133]



(a) SEM image for Ag wire for electrical measurements.



(b) I-V characteristics and measured resistance (resistances in the bracket are calculated value classical resistance formula) for 10nm thick Ag nanowire in different lengths.

Figure 6.6: Electrical characterisation results for thin Ag wires.

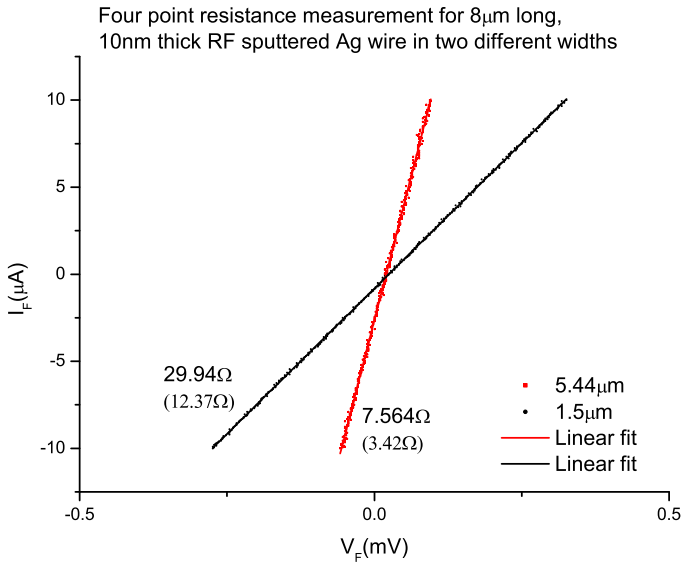


Figure 6.7: Four point resistance measurement result for Ag wire with thickness of 10nm. The resistances in the bracket are calculated using classical resistance formula.

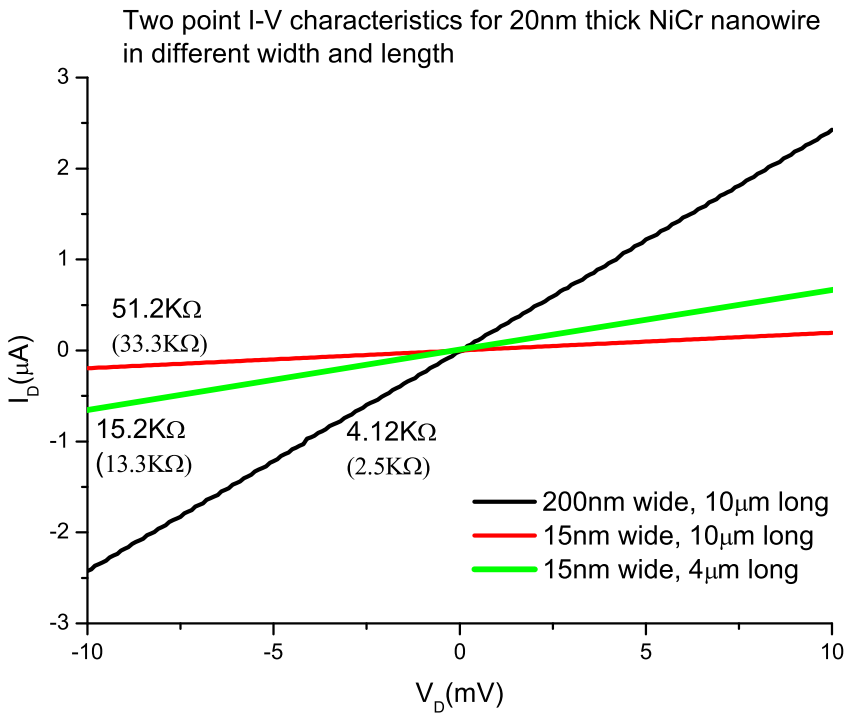
1 to 2 times higher than the calculated mainly due to the grain boundary and surface scattering of thin nanowires.

During the electrical characterisation processes, NiCr nanowires were found to be more durable in terms of current passing capability and more importantly, will not be oxidised at room temperature like Ag and Al. Figure 6.8(b) shows the extraordinary current density capability for ultra thin NiCr nanowire with potential field emission and nanoscale heater for MEMs or lab on a chip applications. The breakdown of nanowire at around 5.5V bias was considered as results of joule heating and electromigration.

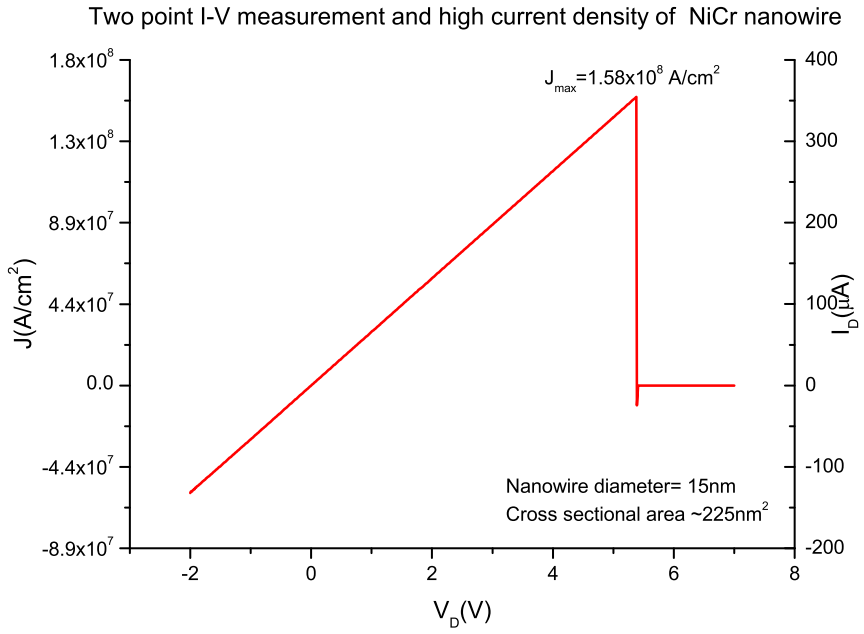
6.3.1 Gate effect measurement of metallic nanowire

6.3.1.1 NiCr nanowires

To explore the transistor operation of thin metal wires, gate effect measurement were performed. The gate effect experiment of NiCr nanowires was configured using setup as shown in Figure 6.3. Due to the high resistance of these wires, a high current up to 100nA has been used. Figure 6.9(a) shows the SEM image and the result of gate effect measurement for a 26nm wide NiCr nanowire



(a) I-V characteristics for 20nm thick NiCr nanowire in different width and length, resistances in the bracket are calculated value using classical resistance formula.



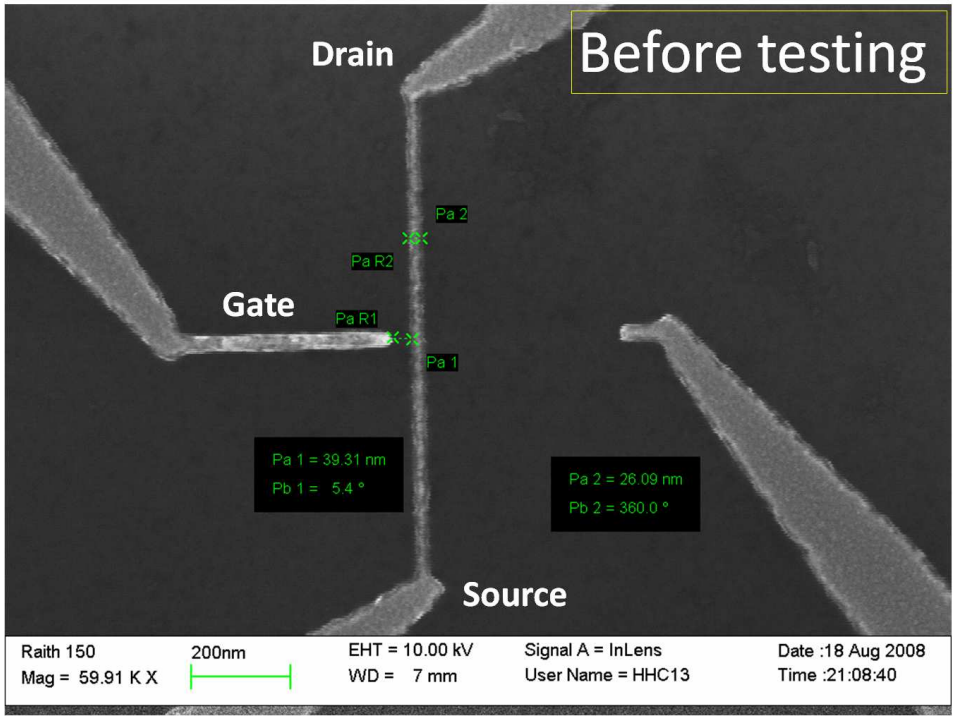
(b) Current density failure analysis for Nichrome 15nm in diameter, achieving a maximum current density of 1.58×10^8 A/cm^2 before breakdown.

Figure 6.8: Electrical characterisation results for NiCr nanowires using HP4155A semiconductor parameter analyser.

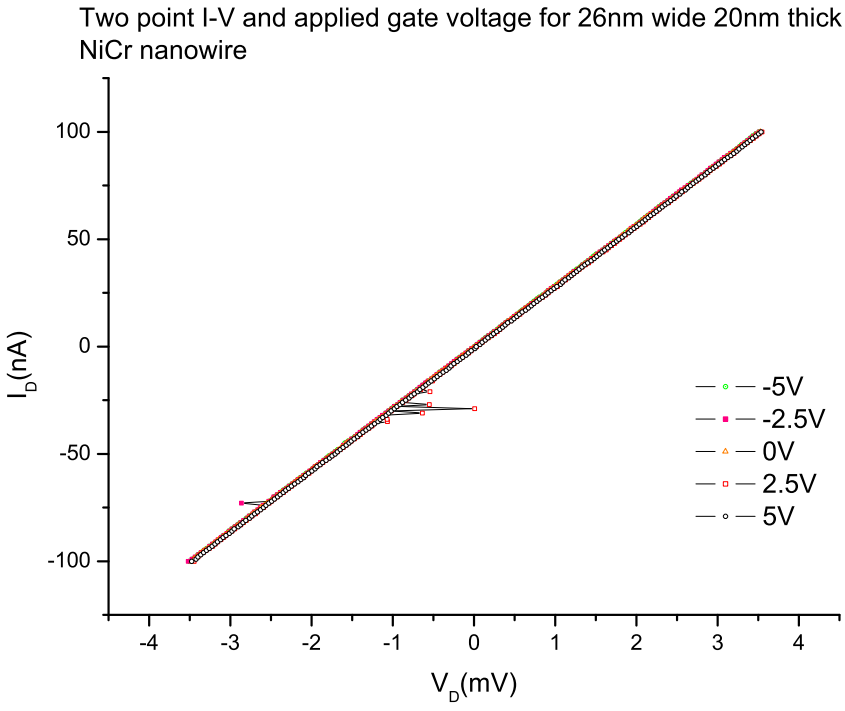
based transistor structure, with applied gate voltages ranging from -5V to 5V. From Figure 6.9(b), it is clear that no electric field effect on current conduction was observed as expected. The nanowire was found to become open circuit after repeating same experiment twice. By taking the sample back to SEM for imaging, the wire was found discontinuous (see Appendix C).

6.3.1.2 Ag nanowires

Similar experiments have been carried out using Ag nanowires. The electric field effect experiments were carried out using the setup shown in Figure 6.3. Due to the low resistance and very fragile nature of these wires, constant current of 200pA was used. The external gate voltages were modulated from -5V to 5V while leakage current being monitored throughout the whole period. Due to the weak screening of Ag, in most of the nanowire samples, electric field effect was not observed. Our previous work[12] indicated some of the samples were found to respond in a switching like behaviour under external gate voltages as shown in Figure 6.10. The experimental result indicated a 60% reduction in drain currents observed at -4V. The gate leakage was found to be around 25pA without the applied field, and increased to around 40pA when -3.5V was applied to the gate. We have also observed the reduction in leakage current when source current the source current is increased, possibly due to the increased in signal to noise ratio of current metre of SMU. Controversy exists on whether the fabricated nanowire was indeed made of pure of Ag, silver oxide (see Appendix B), or have some impurities introduced during the thermal evaporation process, resulting in defects in the ultra fine conduction channel that might be attributed to the observed gating effects. Generally speaking, electric field effects in metals should not be observed under normal condition unless the channel width are few nanometers in scale.



(a) SEM image taken at 59,910X showing a 26nm wide NiCr nanowire structure with one gate located 39nm from the wire before EFE testing.



(b) Influence of applying gate voltage of -5V to 5V on a 26nm wide, 20nm thick NiCr nanowire structure.

Figure 6.9: The SEM image and EFE measurement of a 26nm wide NiCr nanowire structure.

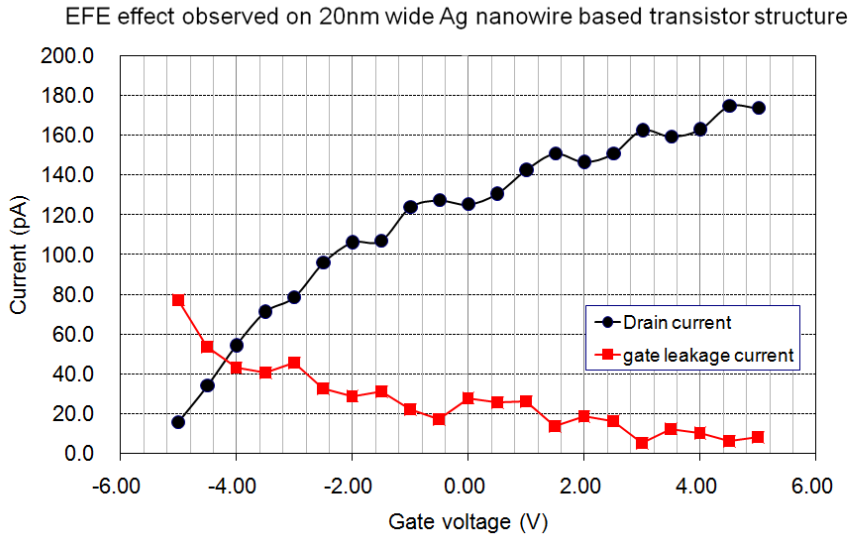


Figure 6.10: Electric field effect observed in 20nm diameter Ag nanowire, carried out in Al shielded box using HP4155 semiconductor parameter analyser[12].

6.4 I-V characteristics of Bismuth nanowires

The semimetal Bi films were milled into nanowire and nanowire based transistor structures using focused ion beam as illustrated in Chapter 5. Due to the thick native oxide of Bi film, Pt nanowires were deposited along with the mill-and-fill process for forming ohmic contacts to sub 100nm Bi wires as illustrated previously in Figure 5.19. For Bi nanowire with widths greater than 200nm, Bi thin films were deposited over the contact electrodes and formed into Bi nanowires structure by FIB milling. Here, we should first present the electrical characterisations of Bi nanowires with larger widths (>200nm) where mill-and-fill processes were not required for ohmic contacts. In this study, a probe station and Keithley 4200 semiconductor parameter analyser with similar setup to the HP4155A shown in Figure 3.11 was employed for electrical characterisations for Bi nanowire based structures.

Figure 6.11(a) shows the FIB milled Bi nanowires with widths ranging from 200nm to 1μm. Due to the large dimensions of these wires, they were fabricated by first evaporating 50nm thick of Bi through an EBL patterned PMMA window on top of SiO_2 substrate with pre-defined Au contacts. The film was deposited directly on top of the gold electrodes and then milled into nanowire structures

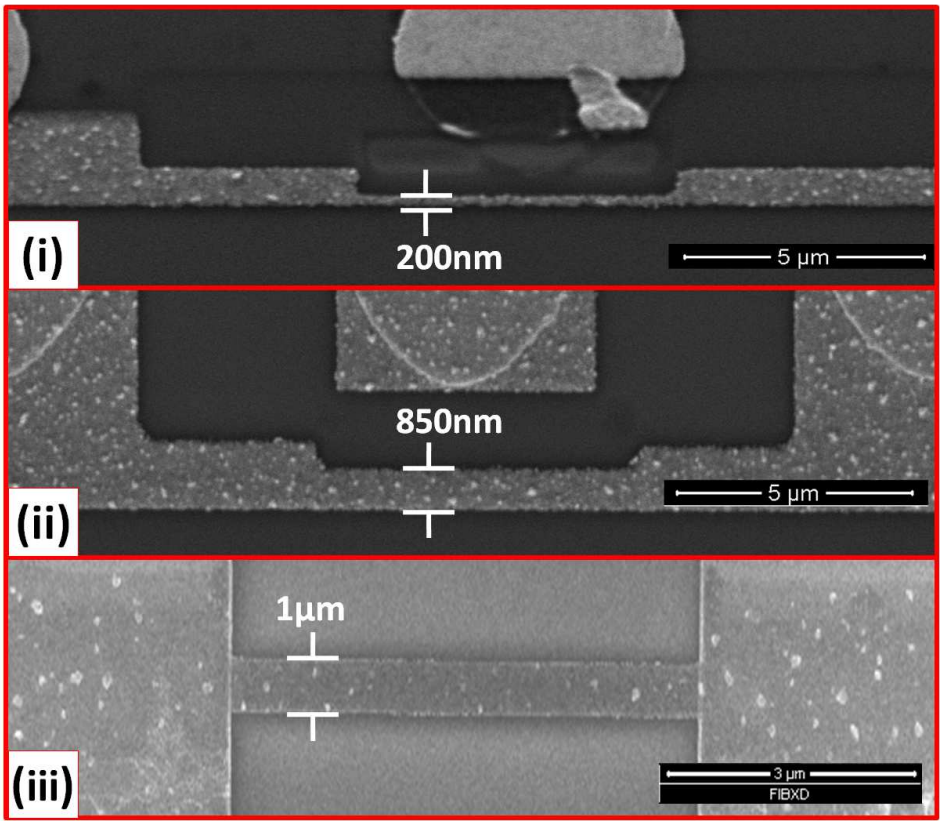
in FIB in the required dimensions. The I-V characteristics indicate ohmic contacts for the Au contacts to the Bi nanowires as shown in Figure 6.11(b). The resistance of these nanowires was found to be four times larger than the calculated value based on bulk resistivity (ρ=1.29$\times 10^{-6}\Omega$m [135]) plus the contact resistances. The abrupt increase in resistance may be contribute from the grain boundary and surface scattering as EMFP of bulk Bi is 100nm, two times larger than the wire thickness. It may also come from the presence of Bi oxides or the ion beam induced implementation of Ga^{+} ions.

In order to determine the contact resistance of these structures, a four point resistance measurement was performed on a 200nm wide Bi nanowire structure. The I-V characteristic of this nanowire can be found in Figure 6.12. The result contains a significant amount of noise. The average resistances were therefore obtained by fitting the curve using linear fitting function in Origin pro 8[136], a data analysis and graphing software. The reason for the level of noise was considered to come from the poorer resolution of large current (>250μA) sourcing at this scale, where the resolution of current and voltage meters lies in the scale of 100nA and 200μV respectively[129]. These noise levels are semi-periodic with frequency of about 0.1V and amplitude of 10pA. Despite the level of noise, the contact resistance on each end of the nanowire was determined to be around 120Ω[‡].

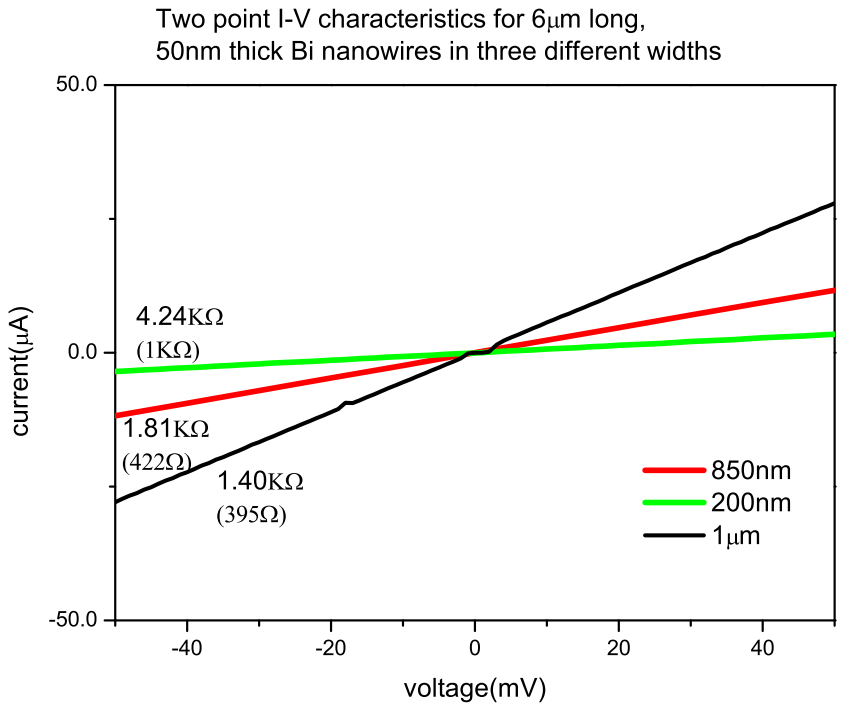
6.4.1 Sub 100nm Bi nanowires

Next, we shall look at the I-V characteristics of 50nm wide Bi nanowires as they are of the greatest interest in this project. Ideally, the size dependent semimetal to semiconductor transition of bismuth will allow us to fabricate single layer and planar transistor structure with drain-and-source channel formed by semiconducting Bi nanowire (<52nm wide) and controlled by semimetallic (>52nm wide) Bi gates and contacts. From our experimental results, for a 50nm wide Bi nanowire, mill-and-fill process must be performed to form improved contacts. Without any oxide removal treatment of Bi nanowires at this dimension, the

[‡]This value can be approximated by first subtracting the four point resistance of 200nm wide nanowire from its two point resistance values, then divide by 2 for each contact.



(a) SEM images taken in FEI-200 FIB system showing Bi nanowires with widths of: (i)200nm (ii)850nm (iii)1μm.



(b) Two point I-V characteristics for Bi wires with widths ranging from 200nm to 1μm.

Figure 6.11: Electrical characterisation results for larger Bi wires.

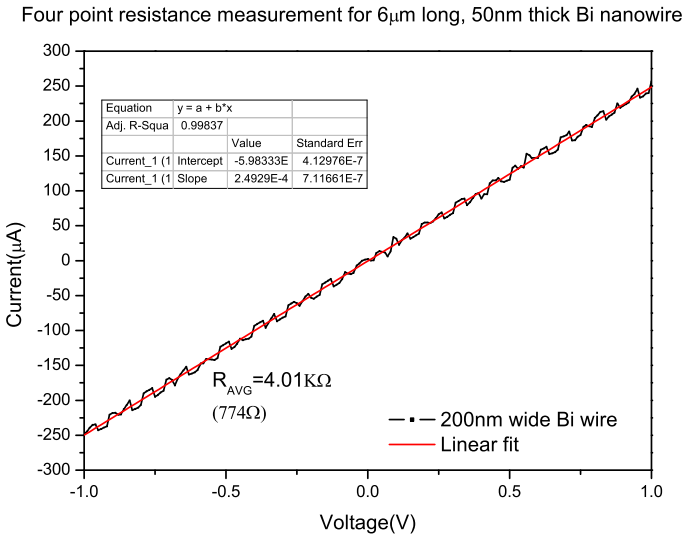


Figure 6.12: Four point I-V characteristics for Bi wires with width of 200nm.

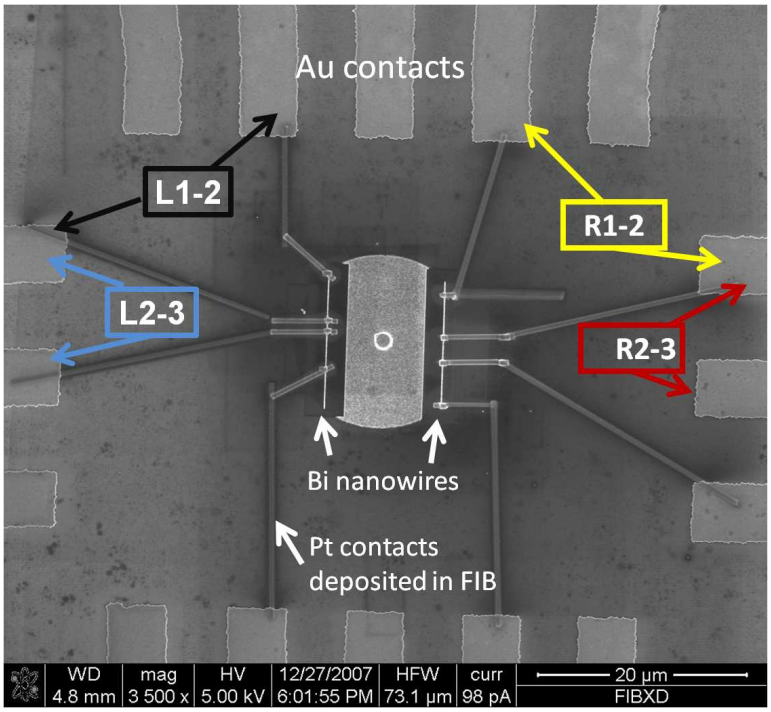
I-V characteristics can become either non-linear or open circuit. Figure 6.13(a) shows SEM image of two 50nm wide Bi nanowire structures milled from the 50nm thick thermally evaporated Bi thin film. The time taken for the deposition of each Pt contact was roughly 70 minutes, and the I-V characteristics of these two wires were carried out using Keithley 4200 semiconductor parameter analyser and probe in aluminium shielded box using the two point resistance measurement setup as in Figure 6.1. The measurements were taken from electrodes based on the denoted area as shown in Figure 6.13(a), and the I-V characteristics of sections of 50nm wide Bi nanowires are given in Figure 6.13(b). Due to the time constraints and FIB availability of the experiments, only a few number of sub 100nm diameter nanowires were successfully characterised. The measurement in Figure 6.13(b) was only carried out in the positive domain and no useful data was obtained at sub 25pA current.

Nanowires with mill-and-fill treatments were found give improved contact resistances. The resistance of these wires were found to be as high as 1.4GΩ, much larger than the reported values from other groups[9][137]. To justify whether these nanowires were indeed improved contact or open circuit, their I-V characteristics were plotted against an open circuit result, taken from one pair of isolated electrodes on the same sample. By comparing the result with the

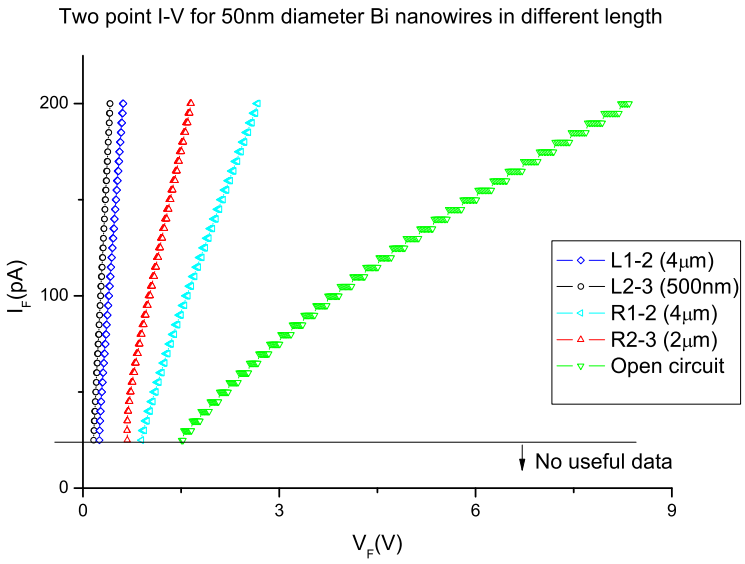
open circuit behaviour, the I-V characteristics of these wires were much lower in resistance and yet linear comparing to the open circuit result. The huge increase in resistance might be the results of a number of factors including the contact resistance from E-beam induced depositions, the surface scattering, grain boundary scattering, and severe ion beam damage during the milling or mill-and-fill process. Among these factors, the most significant contributions were considered to be the ion beam damage and poor conductivity of FIB deposited Pt electrodes[138].

6.4.2 Gate effect measurement on Bi nanowire

Due to the difficulty of fabricating high quality and conducting 50nm Bi nanowires, gate effect measurements have only been carried out on nanowires with widths greater than 200nm. Figure 6.14(a) shows the SEM image of the layout for gate measurement on a 200nm wide nanowire, where the measurement was performed in Keithley 4200 semiconductor parameter analyser using the setup as shown in Figure 6.3. The two point I-V characteristics for 200nm wide, 50nm thick bismuth in the presence of electric field up to 50V can be seen in Figure 6.14. In the experiment, gate effects were not observed, possibly due to the dimensions of this nanowire structure or the gate is located too far away from the main nanowire.

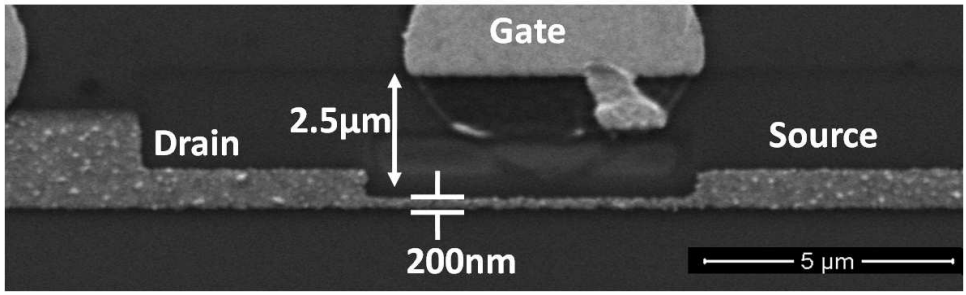


(a) SEM image of two 50nm wide Bi nanowires with FIB deposited contacts (with mill and fill process).

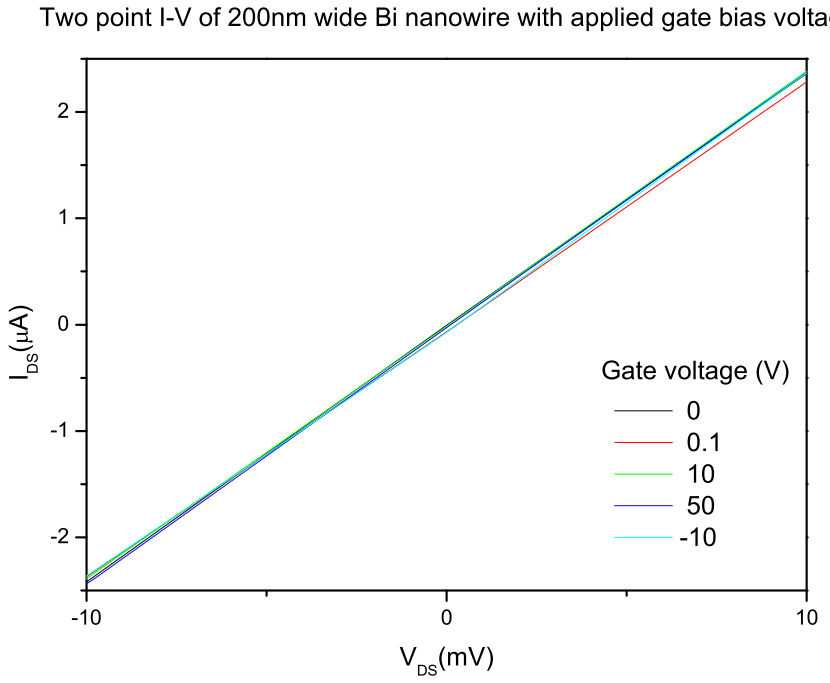


(b) Two point I-V characteristics for each sections of the two Bi nanowires, where the contacts were found to be ohmic to nanowires.

Figure 6.13: (a)SEM image and (b)electrical characterisation results for 50nm diameter Bi nanowires fabricated using FIB milling and having in-situ Pt ohmic contacts.



(a) SEM image of a 200nm wide Bi nanowire fabricated using FIB for EFE measurement.



(b) Electric field effect measurement on a 200nm wide, 50nm thick Bi nanowire, where the gate voltage was varied from -10V to 50V.

Figure 6.14: (a)SEM image and (b)EFE measurement results for 200nm wide Bi nanowires fabricated using FIB milling.

6.5 Discussion

Throughout the fabrication and characterisation process, metallic nanowires have failed to conduct current because of discontinued wires, poor surface adhesion, unsuccessful lift-off, contamination from the metal deposition process, and the spike current caused by the static discharge from the semiconductor analyser[§]. The yield for fabricating devices with all electrical contacts working and carrying measurable current for electric field analysis was found to be relatively low. In fact, among the latest 150 metallic nanowire based transistor structures fabricated in year 2008, only six of them have managed to complete the electric field effect experiment. In most cases, out of the four contacts, only two or three were found to carry current simultaneously, resulting in very low yield of characterisations.

In order to electrically characterise these fabricated thin film and nanowire structures, a number of resistance measurements and gate effect measurement was performed using HP4155A and Keithley 4200-SCS semiconductor parameter analysers. These include two point and four point resistance measurement used to characterise the electrical properties of metallic nanostructures, transmission line measurement (TLM) used to determine the contact resistance, and the electric field effect measurements for exploring the transistor like switching operation on nanowire based structures.

In this chapter, the characterisations of Ag nano stripe structures with very low resistance were first discussed. These measurements have allowed us to study the effect of having one of the dimensions much smaller than the electron mean free path (EMFP), leading to increased resistances due to surface scattering and grain boundary scattering. Zhang[130] simulated the increase of resistivity for Ag films with thicknesses smaller than the EMFP using Fuchs and Sondheimer model (FS model) and Mayadas and Shatkes model (MS model). They found for 10nm thick Ag film, approximately three times increased resistivity in the FS model. Our result from four point resistance measurement agrees closely with their simulation result.

[§]This effect was observed when measuring very low resistance Ag wires with a thickness of 7nm.

Next discussed were the Metallic nanowire structures fabricated using EBL and thermal evaporation based metallisation, where nanowires structure made from Ag, NiCr with widths ranging from 15nm to 200nm have been characterised. Ag nanowires less than 20nm wide were extremely fragile. These wires can blow out after few tests using testing current as low as 100pA-200pA. On the other hand, NiCr nanowires were found to give a much higher success rate for metal lift-off and electrical characterisations. Nichrome nanowires 15nm in diameter were found to be around 1.5 times higher than the calculated resistance using classical approach. Zhang[139] have calculated the stability of metal nanowires at ultra high current densities using self consistent Hartree approximation. In their findings, the highest possible current density that a metal nanowire can sustain is at the $10^{11}\mathrm{A/cm}^2$ range. In our findings, we have explored the current carrying capability of ultra thin NiCr nanowire, where a current density up to $1.58\times10^{8}\mathrm{A/cm}^2$ was achieved before breakdown. This value was truly exceptional as the highest current density for electron transport in a single wall carbon nanotube was found to be at the $10^{9}\mathrm{A/cm}^2$ range[133], one order higher than the 15nm diameter NiCr nanowire.

The exploration of Bi nanowire based transistor structures required profound knowledge of transport properties of the semimetal material. We were able to fabricate Bi nanowires as thin as 30nm structure using FIB as explained in Chapter 5. To understand the electrical properties of FIB milled Bi nanowires, two point and four point resistance measurements were performed. For nanowires greater than 200nm in widths, 5 to 10 times higher in resistances were measured. These results are consistent with Chiu[137] (5 times) for polycrystalline Bi nanowires.

When it comes to electrical characterisation of 50nm wide Bi nanowires, the mill-and-fill process was found to produce linear I-V characteristics, indicating improved contacts from the deposited Pt electrodes to the Bi nanowire structures. Due to the fabrication difficulties involved in making and ohmic contacting Bi nanowires at this dimension, only two point resistance measurement were performed. The I-V characteristics have indicated very high resistance of fabricated structures. From research, Igaki[138] has observed extremely high re-

sistance of Pt contact deposited using electron beam induced deposition in FIB. In their finding ion beam induced deposition can yield lower resistance contacts to their nanostructures. Similar contact resistance values were also observed by Cronin[118], where ion beam induced Pt deposition can result contact resistance as high as 1MΩ. We believe the electron beam induced deposition of Pt contact can contribute significantly to the total resistance for two point measurement and a four point resistance model is required to determine the true resistance of 50nm wide, FIB milled Bi nanowires. Figure 6.15 compares the contact methods employed to 50nm wide Bi nanowires in this work. It is clear that Pt contact to 50nm Bi nanowire with the use of mill-and-fill process has formed the most improved contacts among all other approaches used.

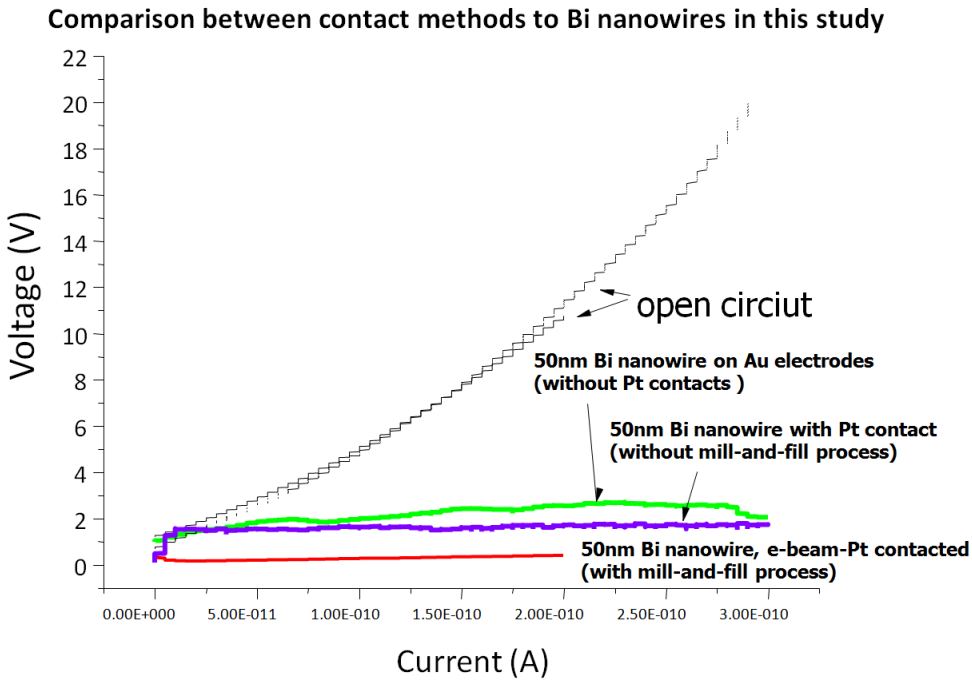


Figure 6.15: Comparison of contact processes of Bismuth nanowire in FIB.

As expected, gate effects of metals were not observed due to our nanowire dimensions. However, in some cases gate effects were sometimes observed in the fabricated metallic nanowire structures, especially more frequently for Ag nanowires[12]. To our knowledge, this could be a result of material deposition contamination, or the defects created during the fabrication process, as the deposition apparatus have been used extensively for all other materials ranging

from metals to semiconductors.

In the four point resistance measurement process, depending on the SMUs used, the I-V results indicated voltage offsets for Ag thin film samples with very low resistance, as shown in Figure 6.16. Although the resistances in a four terminal setup were determined by the slope, the voltage offsets represented the imbalanced short circuit voltage for the SMUs when used as voltmeters. By measuring each of the SMUs for possible voltage offsets, we have found two of the SMUs on the manipulator have offset values as high as 80μV. This voltage offset problem was later minimised by placing the two SMUs with most similar offsets as the voltmeters, while putting others with high offset values as source and ground.

The testing current was also found to be dependent on the measured resistance, especially for low resistance wires. Figure 6.17 shows the effect of testing current level to the measured resistance for sensitive devices. The resistance values were plotted in real time using a four point resistance setup, where 100μA was found to give higher and yet, more stable resistance output than the 10μA source. Moreover, among all four point measurement results, the I-V graphs contains a certain level of noise, possibly due to the imbalanced SMUs used as voltmeters, the resolutions for these SMUs, or the small voltage drop across the wire when a low resistance wire was being characterised.

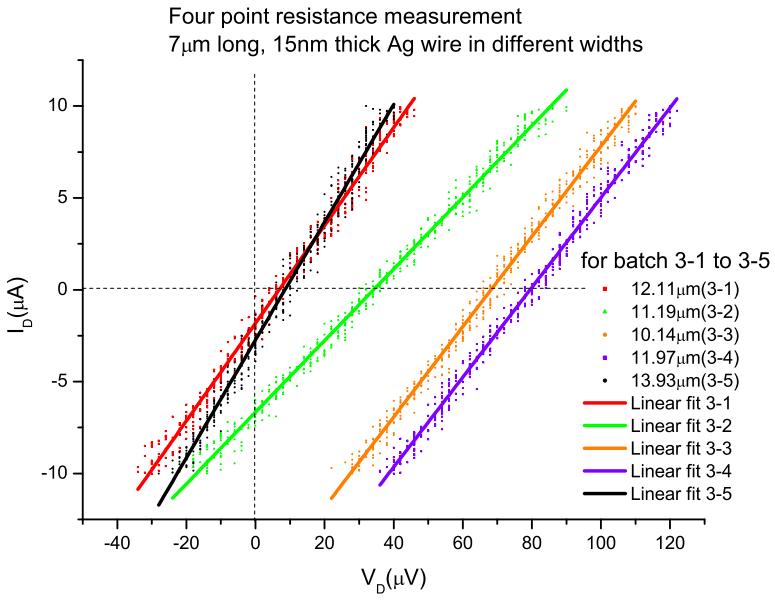


Figure 6.16: I-V characteristics of silver wires with low resistances. The voltage offsets were observed frequently.

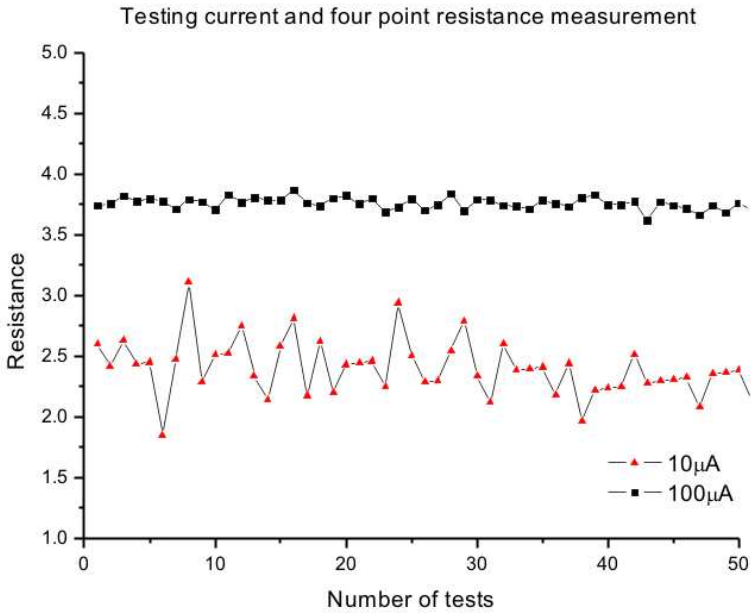


Figure 6.17: Low resistance, and high sensitivity I-V measurements where testing current level can affect the results.

Chapter 7

Conclusions and future work

The continuous scaling down of MOS transistors have shaped and influenced the IC industry. In order to meet the demands for delivering higher performance computers, transistors based on new type of materials or structures must be researched. The aim of this study is to explore and to develop a platform for studying the conduction and gating effects of nanowire based transistor structure with the potential as building blocks for next generation integrated circuit devices.

In this chapter a summary will be given to emphasis main results obtained and the reader is referred to conclusions and detailed discussions in relevant chapters.

The proposed metallic nanotransistor structure is a one dimensional planar device consisting of an ultra narrow metallic nanowire channel, 10-20 nm wide with lateral gate structures separated by 20nm-40nm of air gaps depending on material used. The current work has utilised electron beam lithography and focused ion beam lithography for developing a platform suitable for the fabrication and characterisation of metallic nanowire based transistors with a channel width in the sub 20nm regime. The planar nature of these structures enables nanoimprint technology to be employed in terms of efficient low cost devices suitable for mass production replications. The platform will also allow the characterisations of larger number of devices using systematic and repeatable approach.

During the EBL patterning of the nanowires and nanowire based transis-

tor structures, challenging issues such as surface charging and proximity effects have been encountered. To address these issues, the exposures were performed using low 10KeV of acceleration voltage and the contact pad patterns were designed in a way that covered most of the areas of the insulating substrates to minimise surface charging during the E-beam exposure process. The use of thin PMMA and single pixel line exposure to define isolated areas have reduced proximity effect and enabled sub 15nm wide nanowires to be fabricated with lateral gate structures separated by gaps ranging from 20nm to 200nm. In order to push the minimal linewidth of metallic nanowires into the 12nm scale, the nanowires were defined using single pixel lines with 20nm step size, and developed in an ultrasonic assisted environment.

In the present work we have developed and fabricated nanowire based transistor structures using transition metals, alloy and semimetal materials including Ag, Al, NiCr, and Bi. Two nanowire configurations were investigated , a planer wire with lateral gate electrodes and a Y shaped structure with one gate placed close to each branch. The choices of metals were made based on the fabrication and metallisation process, the oxidation and adhesion issues, the electrical conductivities, and the potencies of electric field effects. The minimum linewidth of 12.5nm NiCr wire was achieved using low acceleration voltage of 10KeV to minimise charging effects, single pass line to minimise proximity effects , 10μm aperture, and a 20nm step size . To our knowledge this is the smallest feature that has been successfully patterned directly on insulating substrates using the Raith-150 EBL system.

FIB has been employed for the development of Bi nanowire based transistor structures, where Bi nanowires with linewidths as small as 30nm have been defined. A substantial efforts have been spent on improving the contact resistance on sub 50nm Bismuth nanowires. This includes the removal of the 10 nm thick native oxide layers and the development of the in situ mill-and-fill process for oxide removal and ohmic contact deposition. Electrical characterisation results (Figure 6.15) have indicated improved conduction for nanowires with mill-and-fill treatments.

In addition to the development of Bi nanowire devices, we have investigated

the potential for direct deposition of highly ordered platinum nanodots on substrates using FIB. It has allowed us to create metal dot arrays with 40-100nm in diameter on Si_3N_4 substrate with a potential storage density of up to 250Gb/in^2. The capabilities of forming 3D multilayer stack of alternating metallic dot arrays have been demonstrated for the first time using FIB as illustrated in Chapter 5.

The characterisations of the nanowire structures were performed using semiconductor parameter analysers with micro manipulators This allowed the study of the electrical properties of different metal nanowire structures deposited on insulating substrate. As previously described in Chapter 6, nanowires made from Ag, NiCr, and Bismuth have been electrically characterised with measured resistances ranging from few ohms (thin Ag stripes) to 1.4GΩ (FIB milled Bi nanowire). The resistances of nanowires are found to be few times higher than their bulk resistances mainly due to the effect of grain boundary and surface scattering. For sub 50nm Bi nanowires, extremely high resistances were obtained mainly due to the ion beam damage and grain boundary scattering due to the high electron mean free path of bismuth.

In order to explore the potential of nanowire based metallic transistor structures, gate effect measurements were performed by supplying gate voltages in the range from 1-5V through the lateral gate structures and monitoring the drain to source current. Although no significant gating effects were observed due to the diameter of these nanowires (20nm for metals, and 200nm for bismuth) being one to two order larger than their screening depths (few angstroms for metals and 40nm for bismuth), the fabrications of these devices have allowed us to explore the resolution limits of EBL and FIB based processes in depth as covered previously in Chapter 4 and Chapter 5.

7.1 Thoughts for future works

7.1.1 Nanoimprint mold fabrication

The low yield and great difficulty involved in fabrication and characterisation of metallic nanowire devices can be improved by employing replication technologies such as nanoimprint. Mohamed[13] had previously developed the process of master mold making for nanowire based transistor structure using NiCr as etch mask during the reactive ion etching process of quartz substrates. This allows the use of UV-assisted imprint process for high resolution pattern transfer. Figure 7.1 shows the SEM image of a quartz nanoimprint mold made using EBL and RIE with CHF_3, where NiCr was used as etch mask[13].

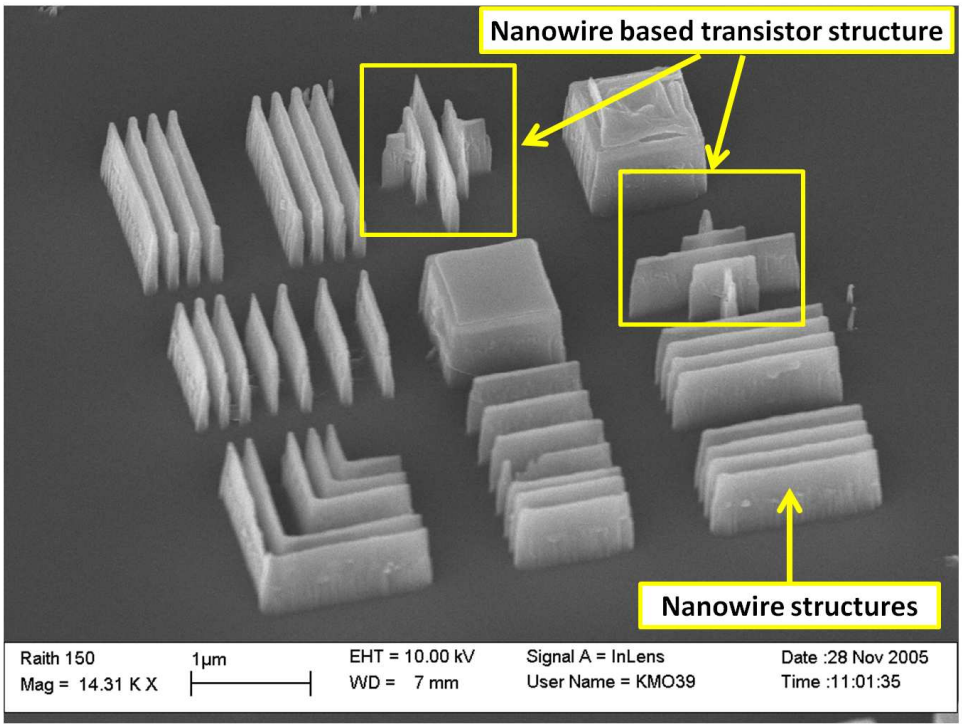


Figure 7.1: SEM image showing a quartz mold containing 45nm wide nanowires and transistor structures with gates separated by 100nm of gaps from the main nanowires[13].

7.1.2 Characterisation improvements

In terms of electrical characterisation of these devices, high-k dielectric materials can be employed to further reduce gate leakage, and also allow the electric field

penetration to become more observable based on Black's prediction[7]. The use of high resolution SMUs (HRSMU) will also improve the resolution of I-V or EFE measurements[129]. Moreover, transistor with back gate structures can also be utilised for a high voltage gate effect measurement by employing a double sided Si wafer or etch into the insulating substrate for Si substrate contacts.

7.1.3 1D PEDOT nanowire transistor

As previously mentioned in Chapter 5, PEDOT is a conductive polymer suitable for acting as charge dissipation layer during FIB milling process. Mohamed[13] has studied the effect of electron beam irradiation of PEDOT in EBL. PEDOT can be utilised to form ultra narrow nanowire structures by single pixel line exposure in EBL. Unlike metals, PEDOT can be coated on insulating substrates using spin coating, and for the unexposed regions, can be removed by DI wafer. The resolution of patterning PEDOT depends only on the beam spatial distribution and the polymer bonding properties of the material as it does not require any development process. As a result, one can patterning nanowire features on this conducting material by employing 30KeV of acceleration voltage, 10μm of aperture, 25pA of beam current, 25μm of write field, with potential of achieving sub 10nm resolution.

7.1.4 Nanoimprint or focused ion beam assisted 1D graphene transistor patterning

Due to the fabrication difficulties involved for creating metallic nanowires in the sub nanometer scale, semimetals that have been studied extensively in this decade, can be utilised to demonstrate the electric field effects at much larger dimensions. For semimetals, electric field effects have been demonstrated on both Bi and 1D graphene layer[37]. Unlike bismuth, graphene can be easily made into mono-layer, suitable for transistor operations. It is our belief that by employing focused ion beams of graphene milling, it could be integrated into sub 30nm transistor structures, with a channel thickness of just one monolayer. Moreover, depending on the surface energy of graphene, it could be suitable for

high density, large area integration using nanoimprint technology.

7.1.5 Nano heater structure

In chapter 6.3 we have presented the ultra high current density capability of NiCr nanowires. With this current density, NiCr wire was found to sustain a dissipation power up approximately 1.9mW. As a result, one can implement NiCr nanowires in an arrangement (Figure 7.2) that might be useful for application when localised heating is desired such as biochips, lab on a chip, MEMS and NEMS devices. This kind of structures can be defined using EBL with similar exposure parameters suggested for high resolution EBL patterning as in Chapter 4.3.3.

Figure 7.2: A simple structures for nanoscale heater layout (not to scale). Where line width as small as 20nm can be fabricated using EBL based processes.

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Appendix A

Publications

1. H. H. Cheng, J. K. Siaw, and M. M. Alkaisi, "The fabrication of metallic nanotransistors," Conference on Optoelectronic and Microelectronic Materials and Devices, CMMAD, IEEE Press Proceedings, pp. 121-124, 2004.
2. H. H. Cheng, C. N. Andrew, and M. M. Alkaisi, "The fabrication and characterisation of metallic nanotransistors," Microelectronic Engineering., vol. 83, Issues 4-9, pp. 1749-1752, 2006.
3. H. H. Cheng, Shang-En Wu, M. M. Alkaisi, and Chuan-Pu Liu, "Fabrication of bismuth nanowire devices using focused ion beam milling," Advanced Materials and Nanotechnology AMN-4, AIP Conference Proceedings 1151, pp. 48, 2009.

Appendix B

Oxidation of silver nanowires

Without dielectric coatings, Ag nanowire structures can be oxidised in room temperature in air. The following figure shows an Ag nanowire structure after exposing to air for three weeks. It is clear that oxides were grown on Ag nanowires forming grain like features.

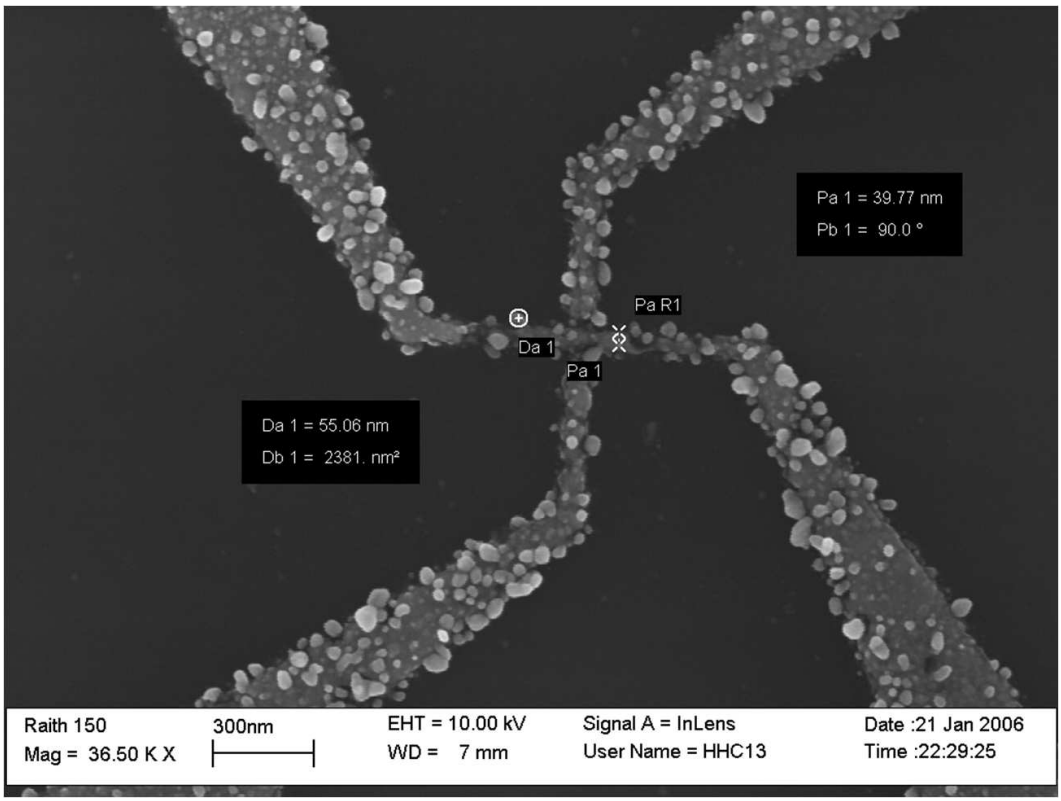

Figure B.1: SEM image showing self-oxidising of Ag nanowire structures exposed to air for a period of three weeks.

Appendix C

Breakdown of nanowires during electrical characterisations

Sub 20nm wide nanowires were found extremely fragile during the I-V and EFE characterisations. Figure C.1 shows the SEM image of a 26nm wide NiCr nanowire after two times of EFE measurements. The wire was found to become discontinuous under the SEM.

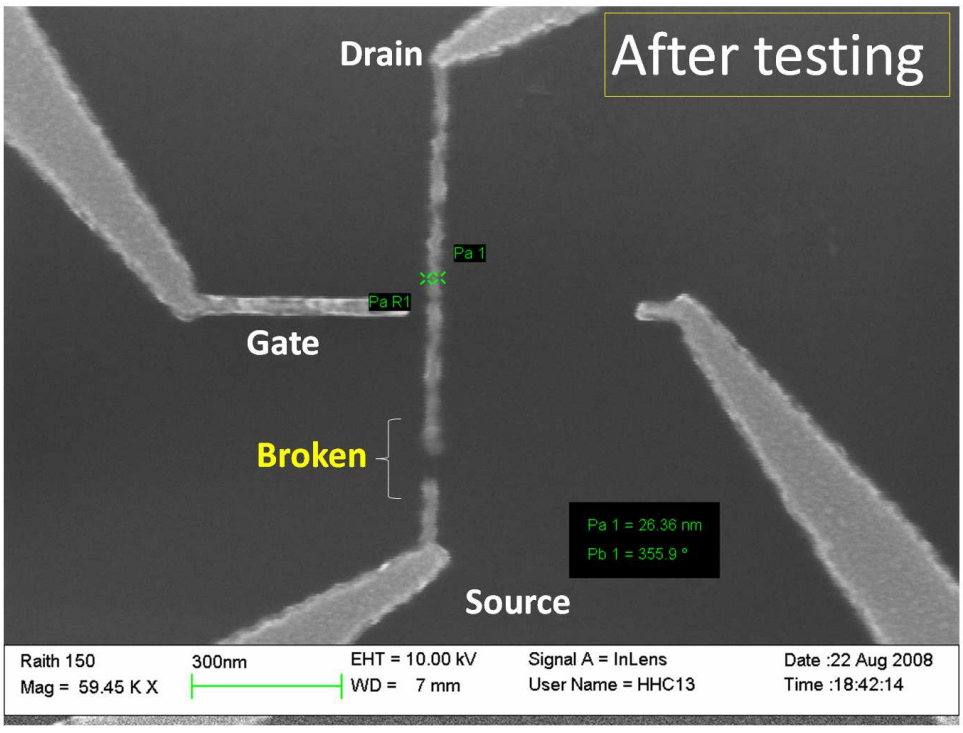

Figure C.1: SEM image showing a section of broken nanowire after EFE measurements.

The figure below shows SEM image of NiCr nanowire after performing high current density test as in Figure 6.9.

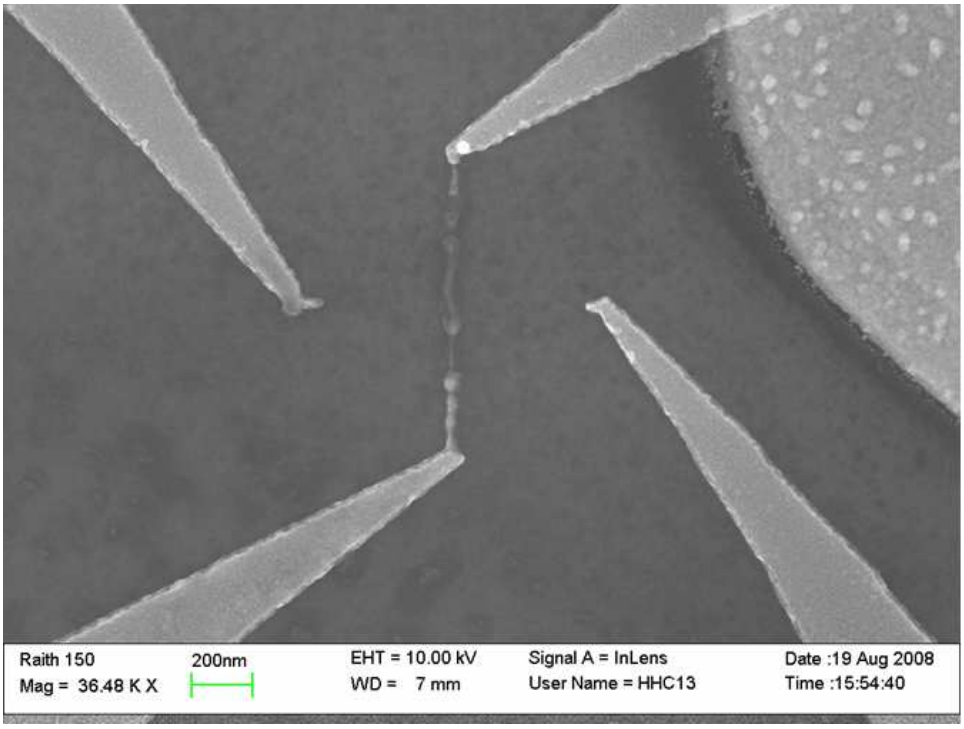

Figure C.2: SEM image showing a broken and molten NiCr nanowire after performing high current density measurement with up to $1.59 \times 10^8 \mathrm{A/cm^2}$ of current density